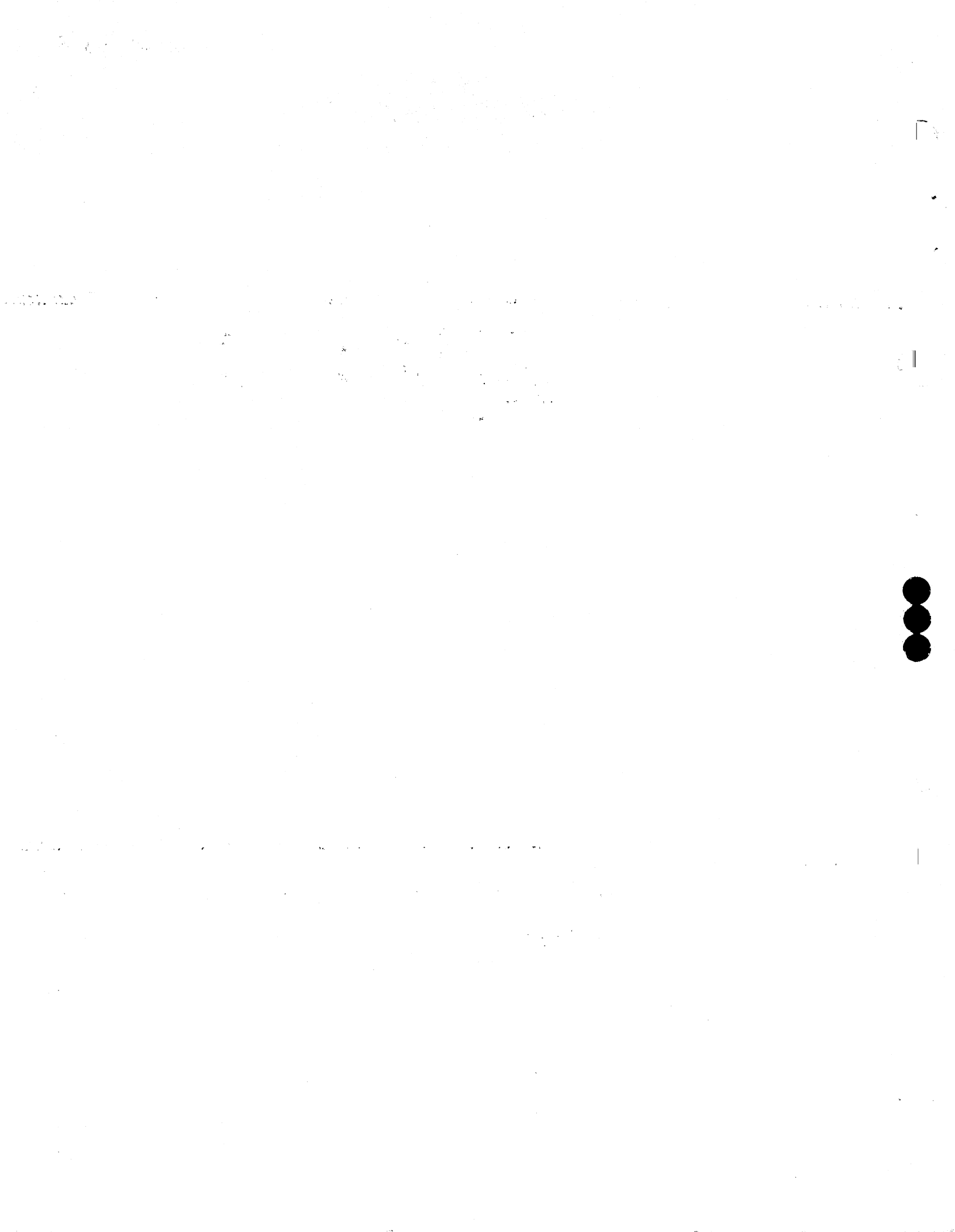




**OPERATIONAL DIAGNOSTIC
SYSTEM (ODS) VERSION 1
REFERENCE MANUAL**

CDC[®] COMPUTER SYSTEM

CYBER 18-05





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LIST OF EFFECTIVE PAGES

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PREFACE

This manual describes the capabilities and operation of the Control Data® Operational Diagnostic System Version 1 (ODS) maintenance software diagnostic package. ODS Version 1 is to be used as a maintenance and checkout tool to identify and isolate any failures in the replaceable subassemblies of the CYBER 18-05 Computer Systems with CORE memory. It is suggested that this manual be used in conjunction with the hardware maintenance manual for the appropriate system being tested.

This manual has been designed to lead the reader logically through the steps that are required for using the ODS diagnostic tests for maintenance and checkout of hardware equipment. Sections 1 through 5 give the reader introductory information as well as loading, test control, run parameter, overlay structure, operator command, and error handling information. Sections 6, 7, and 8 cover the LODCHK program and level I and II

test information. Section 9 covers the multiplex tests for limited memory configurations. A glossary, a list of routines available to the ODS system, deadstart format, and absolute binary card format information are supplied in the appendixes. It is suggested that the reader becomes familiar with the terms in the glossary before reading the manual.

This manual is intended for a customer engineer with a working knowledge of CYBER 18 Computer Systems.

Part numbers are supplied for all tests and for special data decks so that decks can be identified and reordered by name or number.

For further technical information the following manuals are suggested:

<u>Title</u>	<u>Publication Number</u>
CYBER 18 Processor with Core Memory (Macro Level) Reference Manual	88973500
CYBER 18-05/10 Computer Systems Hardware Maintenance Manual, Volumes 1 and 2	96767500 96767600



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The Operational Diagnostic System (ODS) is a software diagnostic package that, in conjunction with the appropriate hardware maintenance manuals, provides a complete maintenance system for the micro processor and the various peripherals connected to it.

FEATURES

ODS, when used in conjunction with the hardware maintenance manuals, offers the following features:

- Ability to detect and isolate failures to the replaceable subassemblies
- Ability to run in a minimum of 8K macro memory
- No ODS termination due to hardware failure other than hardware nucleus required to load and execute diagnostic software
- Action codes referencing entries in the diagnostic decision logic tables (DDLTs) in the hardware maintenance manuals
- Concise English-text error messages as well as informative messages
- Programs written in higher level language
- Structured format design

SOFTWARE

The ODS software is composed of three types of diagnostics that require different loading procedures. The three types are:

- Loadcheck (LODCHK)
- Level I diagnostic tests
- Level II monitor and diagnostic tests

Individual ODS test diagnostics are described in detail in section 6 (LODCHK), section 7 (Level I Tests), and section 8 (Level II Tests).

Table 1-1 indicates the tests for each piece of hardware tested, overlay structures, and pertinent comments for the different tests. Table 1-2 lists the part number for the individual test decks, listings, and utility packages that may be ordered.

LOADCHECK (LODCHK)

LODCHK is a stand-alone deadstart program that performs the following functions:

- Checks the micro instructions by executing a selected set of macro level instructions
- Checks the lower half of stack zero memory (lower 4K)
- Checks the load path
- Checks the conversational display terminal (CDT)
- Loads level I programs and/or the level II monitor

LODCHK must always be the first ODS program loaded.

LEVEL I TEST DIAGNOSTICS

Level I diagnostics are stand-alone diagnostic tests in 12-bit absolute binary format. The level I programs do not require a monitor and execute independently of all other maintenance software programs.

Level I consists of the following diagnostic tests:

- MPINS — Instruction set tests
- MPMEM — Core memory tests
- MPRTC — Protect system tests
- LIAT2 — LIAT model II conversational display terminal (CDT) and model III keyboard tests
- CRECO — Card reader/line printer controller tests

TABLE 1-1. SYSTEM TEST OVERVIEW

Equipment Tested	Test Mnemonic	Action Code ID†	Program Diagnostic Level	Number of Test Sections	Comments
Micro Processor Load Path	LODCHK	—	I	6	Load level I programs after ensuring that instructions, memory, and load path are functional.
Micro Processor	MPINS	01	I	9	Instruction test
Micro Processor	MPMEM	05	I	5	Macro memory test
Micro Processor	MPRTC	06	I	5	Protect system and interrupt test
CC614 Conversational Display Terminal (CDT)	LIAT2	07	I	9	Comment device
FH301-A Card Reader/Line Printer Controller	CRECO	08	I	4	Echo test
CB104 Card Reader	CR104	11	II	5	300 or 600 cards/minute
	CRUT1	16	II	2	
	CRUT2	17	II	1	
	C104M	18	II	1	
CL408 Line Printer	LP408	12	II	7	300 lines/minute
	L408M	1A	II	1	
Magnetic Tape Subsystem: BW101-A/BW301-A Magnetic Tape Transports, FA107-A Magnetic Tape Controller	LCTTA	13	II	2	NRZI, 25 inches/second, seven-track or nine-track
	LCTTB	14	II	12	
	LCTTM	19	II	2	
FJ441-A Dual-Channel Communication Line Adapter (DCCLA), DCCLA Controller	CLA2A	15	II	11	Two-channel
	CLA2M	1B	II	1	

†Action code ID includes the two left-most digits of the action codes; i. e., 0540 refers to an MPMEM action code.

LEVEL II MONITOR

The monitor is responsible for the complete control of the ODS level II system. It is core-resident and supplied in 12-bit absolute binary format.

The monitor performs the following:

- Standard machine-operator interface

- Loading of diagnostic tests
- Parameter display and entry
- Error handling and reporting
- Control of test execution (section selection, multiplexing, pass count control, repetition of test, section and subsection, halts, number of passes, and abortion of tests)

TABLE 1-2. SYSTEM PART NUMBERS

Part Numbers		Test Deck
Overlay	Non-Overlay	
96820100	96820200	Entire batch system except listing and microfiche
96807500	—	LODCHK
—	96809400	LDCHK2
96807600	96809600	MPINS
96807700	96809700	MPMEM
96807800	96809800	MPRTC
96807900	96809900	LIAT2
96808000	96812500	CRECO
96808600	96813100	CR104
96808700	96813200	CRUT1
96808800	96813300	CRUT2
96808200	96812700	LP408
96808300	96812800	LCTTA
96808400	96812900	LCTTB
96808500	96813000	CLA2A
96808100	96812600	Level II Monitor
96808900	96808900	Read Adjustment Deck
96809000	96809000	Sync Adjustment Deck
96809100	—	Special decks, non-test related. Used in conjunction with the hardware maintenance manuals
96809200	—	
96809300	—	
96809500	—	ODSBOT
—	96813900	C104M
—	96814000	LCTTM
—	96814100	L408M
—	96814200	CLA2M
96814300		MEMDMP Dump Program
96820000		ODS Listing
12314181		ODS Microfiche Listings†

†Microfiche is not part of the SSD-supported material; however, support is provided by ESS and is listed here for the customer engineer convenience.

- I/O message handling
- Interrupt handling
- Utilities (code conversion, random number generation, etc.)

LEVEL II TEST DIAGNOSTICS

Level II test diagnostics are diagnostic tests in 12-bit absolute binary format. Level II tests execute under control of an ODS monitor but without the presence of an operating system. Level II tests allow for multiplexing of tests in the non-overlay version.

Level II consists of the following tests:

- CR104 — 300/600 card-per-minute card reader (CB104) tests
- LP408 — 300 line-per-minute line printer (CL408) test
- LCTTA — Magnetic tape transport controller (FA107-A) tests
- LCTTB — Magnetic tape transport controller (FA107-A) and magnetic tape drives (BW101-A and BW301-A) tests
- CLA2A — Dual-channel communications line adapter (DCCLA) and DCCLA controller (FJ441-A) tests
- CRUT1 — Card reader utility for calibration tests
- CRUT2 — Card reader utility for timing tests
- C104M — Card reader multiplexing test
- L408M — Line printer multiplexing test

- LCTTM — Magnetic tape multiplexing test
- CLA2M — Dual-channel communications line adapter multiplexing test

HARDWARE

The minimum and maximum hardware configurations are shown in figures 1-1 and 1-2, respectively.

The minimum configuration consists of the following hardware:

- Micro processor with 8K of macro memory
- CB104 Card Reader
- FH301-A Card Reader/Line Printer Controller
- CC614 Conversational Display Terminal

The maximum configuration consists of the following hardware:

- Micro processor with 65K of macro memory
- CB104 Card Reader
- FH301-A Card Reader/Line Printer Controller
- CL408 Line Printer
- FA107-A Magnetic Tape Controller
- BW101-A or BW301-A Magnetic Tape Transport
- FJ441-A Dual-Channel Communications Line Adapter
- GH508-A Basic Operators Panel (BOP)
- CC614 Conversational Display Terminal

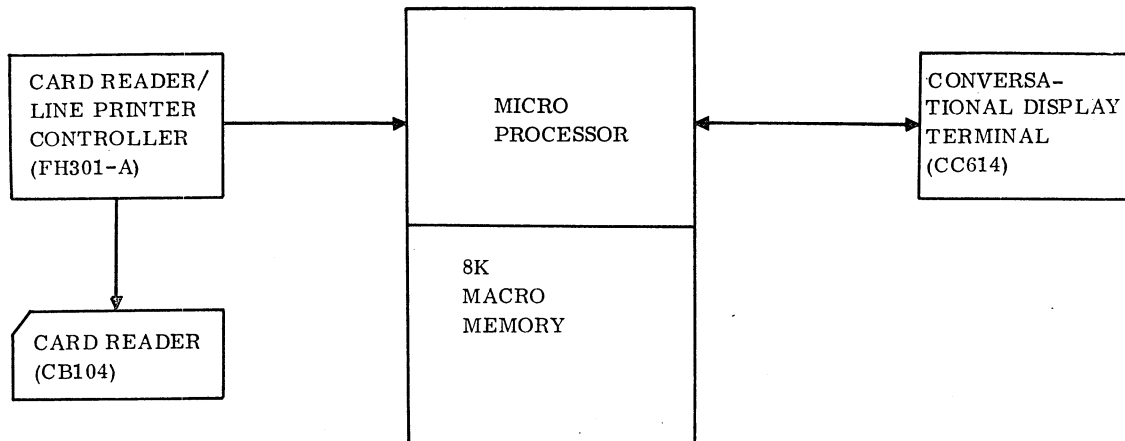


Figure 1-1. Minimum Hardware Configuration

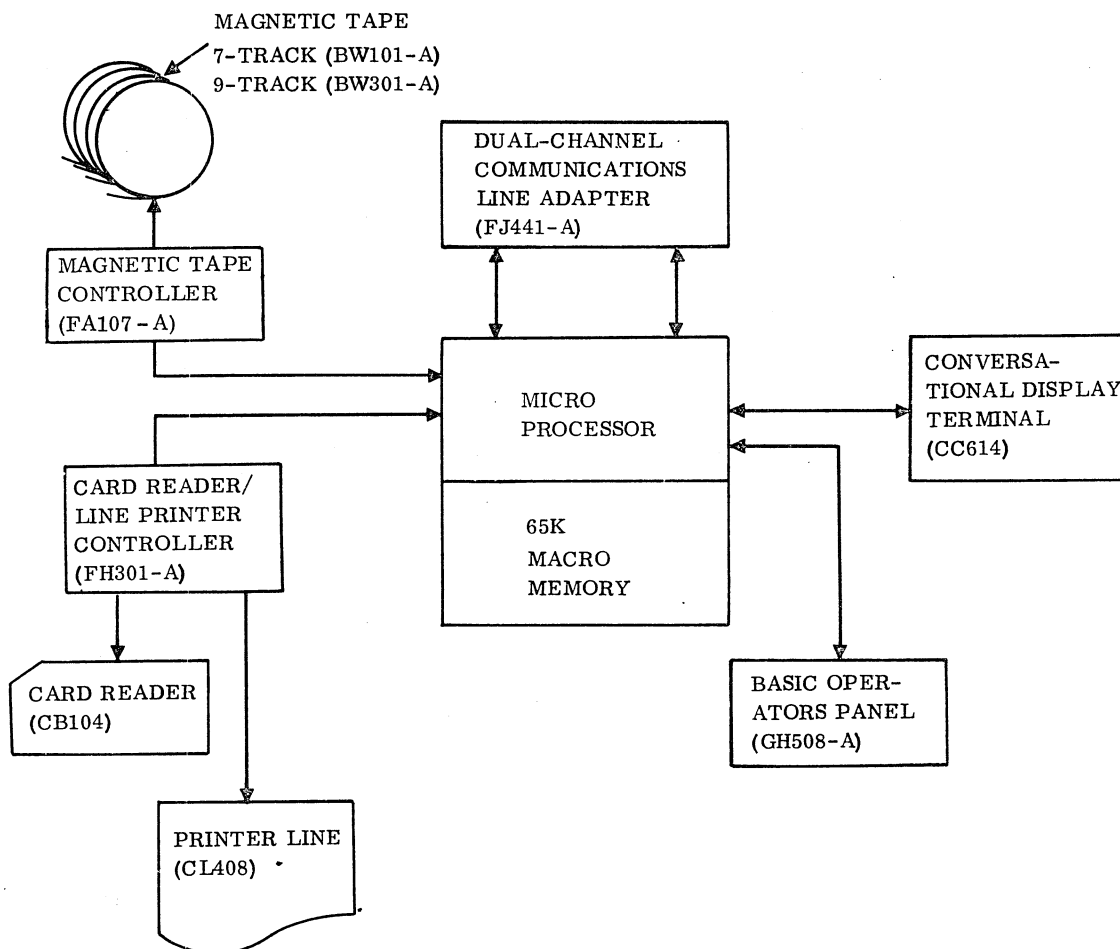
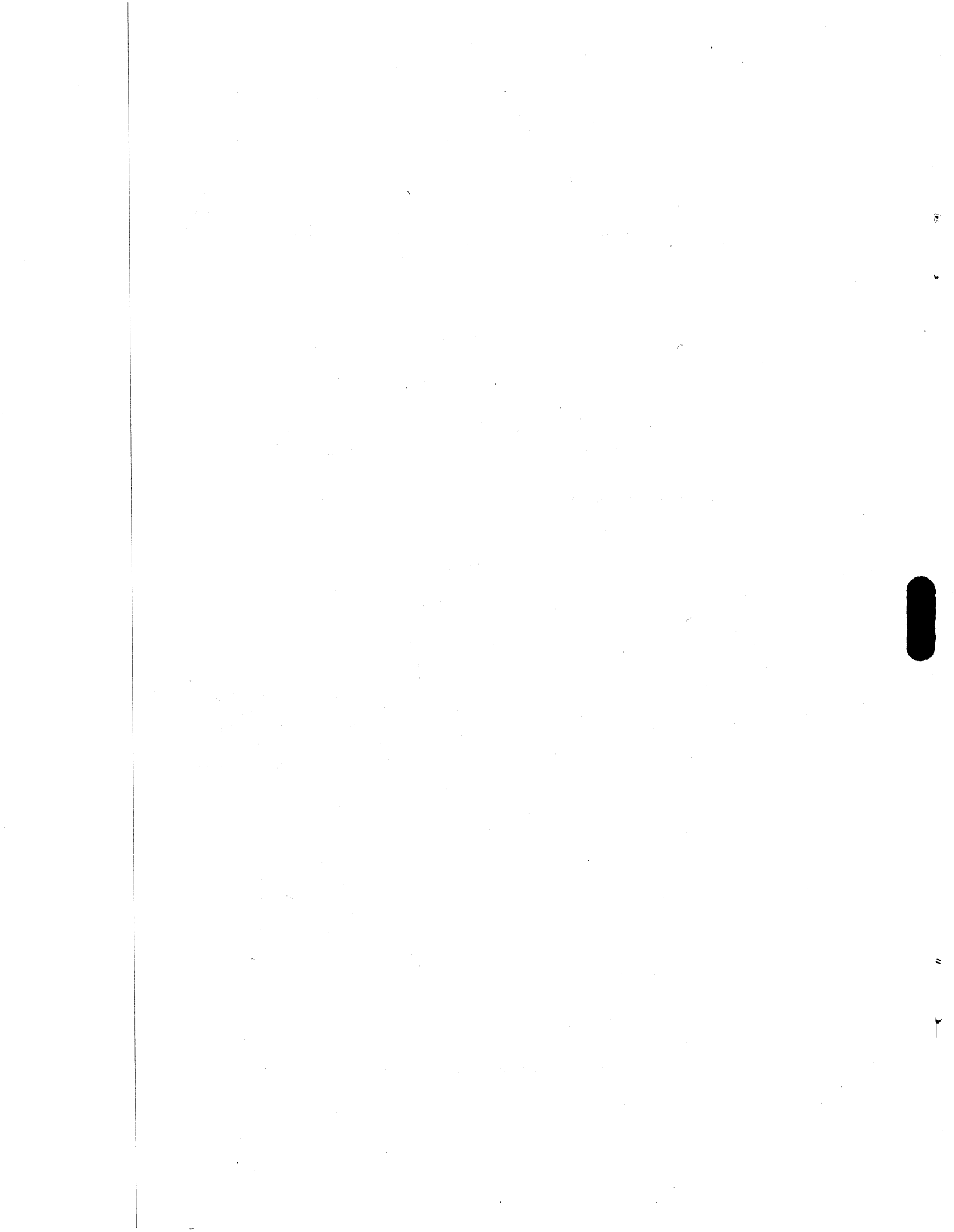


Figure 1-2. Maximum Hardware Configuration



The ODS maintenance software must exist on punched cards, as the CB104 Card Reader is the only load device currently supported by ODS.

NOTE

The loading of LODCHK is a prerequisite to loading any level I program or the level II monitor. In addition, the level II monitor is a prerequisite to load a level II program.

The loading sequence of both the level I and level II test programs may be random.

LOADING PROCEDURES

LODCHK AND LEVEL I TEST PROGRAMS

LODCHK exists in deadstart format[†] and must be the first program loaded into memory. The procedures and methods outlined in table 2-1 are designed to load and execute LODCHK, which in turn loads and executes level I tests. Upon completion of a successful LODCHK load, the system displays 123456 on the conversational display terminal (CDT).

For LODCHK operation, refer to the Loadcheck section (section 6).

ODSBOT LOADING

It is possible to load any level I overlay diagnostic into any of the first four memory stacks (0000, 2000, 4000, or 6000) by using ODSBOT instead of LODCHK.

NOTE

None of the diagnostics run above address 7FFF, even though memory up to 65K is available. The level II monitor and MPRTC must always be loaded at address 0000 in order to execute properly.

To provide the capability to load a level I diagnostic into any stack, ODS supports a program called ODSBOT. This program is provided in deadstart format. The procedure for loading a level I test or the level II monitor with ODSBOT is identical to that described in table 2-1, except that the deadstart deck for ODSBOT is used in place of the deadstart deck for LODCHK. The last 31 cards in the ODSBOT deadstart deck are listed in figure 6-3. These are the level I parameter cards that are also used by LODCHK and may be customized by the operator.

NOTE

The equipment code used by ODSBOT is contained in the second word of these parameters.

The first and last cards of the ODSBOT deadstart deck control the address at which the ODSBOT program is deadstarted into the main memory of the micro processor. The format of the first card is:

```
K 7 1 0 0 8 0 0 0 G K x x x x G
```

The format of the last card is:

```
K x x x x G J 1 0 G K 4 1 2 0 2 8 0 0 +
```

The parameter xxxx on both cards determines the deadstart address and, consequently, the address at which the diagnostics are loaded. Following are the values

[†]For deadstart deck format and setting, refer to appendix C (Deadstart Format).

TABLE 2-1. LODCHK AND LEVEL I LOADING PROCEDURES

Procedure	Methods	Comments
Master clear	<ol style="list-style-type: none"> 1. Press ESCAPE key on the console keyboard 2. Press the SHIFT and ? keys simultaneously 	<p>This puts the CDT into panel mode.</p> <p>If master clear is successful, a question mark (?) is displayed or typed out.</p>
	<ol style="list-style-type: none"> 1. Press the red MASTER CLEAR button on maintenance panel. 	Not all configurations have this panel.
	<ol style="list-style-type: none"> 1. Press the MASTER CLEAR button on the basic operators panel (BOP) 	Not all configurations have this panel.
Prepare and load card reader	<ol style="list-style-type: none"> 1. Place LODCHK and any level I card decks in the card reader hopper. 2. Place card weight on top of the card decks. 3. Press the RESET button on the card reader. 	<p>LODCHK must be the first deck. Level I card decks may be in random order; however, the standard deck sequence is:</p> <p style="padding-left: 40px;">LODCHK MPINS MPMEM MPRTC CRECO LIAT2</p> <p>After pressing the RESET button, check that the RESET light is on.</p>
Read in card decks for deadstarting	<ol style="list-style-type: none"> 1. Move the deadstart toggle switch down; then move it up. 	The toggle switch may be located in different positions for different configurations.
	<ol style="list-style-type: none"> 1. Press the AUTOLOAD button on the basic operators panel (BOP). 	Not all configurations have this panel.
Modify level I test run parameters	See the Level I commands section (section 4)	—

for parameter xxxx to allow loading diagnostics into the various stacks:

<u>Value of xxxx</u>	<u>Load Address</u>
1000	0000
3000	2000
5000	4000
7000	6000

The default xxxx value is 1000, which causes the diagnostic to load at 0000.

ODSBOT detects and reports exactly the same errors during loading of level I tests as does LODCHK. The reporting mechanism employed by ODSBOT uses the selective stop feature of the micro processor with the value in the P register at the time of the halt indicating the detected error. However, since ODSBOT may be loaded in stacks 0 through 3, the loader stop addresses described in table 6-1 match those used by ODSBOT after subtracting the first word address of the stack being loaded into from the value reported in the P register. For example, if ODSBOT is loaded into

stack 3 (FWA=7000) and halts during loading, a level I diagnostic with a value of 7EFA in the P register. Simple arithmetic shows that a sequence error was the problem:

$$7EFA-6000 = 1EFA \Rightarrow \text{Sequence Error}$$

LEVEL II MONITOR AND TESTS

The level II monitor must be the first level II deck loaded after LODCHK or ODSBOT and the level I tests (if any).

It is important to note that there are two ODS monitors for level II. The correct one is chosen on the basis of maximum macro memory in the computer. The two monitors are:

- ODS overlay monitor — This monitor is designed to run in 8K of macro memory. It supports diagnostic test overlays, but does not support diagnostic test multiplexing. It can execute in configuration with more than 8K of memory; however, it uses only 8K of memory.
- ODS multiplex monitor — This monitor is designed to run in a minimum of 16K of macro memory. It supports diagnostic test multiplexing but does not support diagnostic test overlays; however, repeating of tests is allowed.

The monitor is loaded using the same loading procedures and methods as the level I tests described in table 2-1. After being loaded, the monitor displays the following message on the CDT:

ODS x.xx

Where: x.xx is the revision number.

This message also indicates that the monitor is ready to load the level II tests using the procedures and methods outlined in table 2-2.

OVERLAY STRUCTURE

The ODS software must run in a minimum of 8K of macro memory. To meet this requirement, an overlay structure is supported by both the level I executive and level II monitor. An overlay consists of at least one test section.

When a test is loaded, the executive loads only the first overlay. When the test is put into execution, the executive passes control to the test sections in the order they are selected. The executive determines which sections are in the current overlay. If the currently selected section is found, it is executed; if not, the next overlay is read, and so on until the currently selected section is found. When an end-of-file is read, the executive assumes that all overlays have been read and that the selected section could not be found. A section not found message is displayed on the CDT and the system attempts to find the next selected test section.

If the operator requests a section that does not exist for this test, the executive determines that fact and prints a section not found message without searching for the nonexistent section. The executive then attempts to execute the next selected section.

After all selected sections have been handled, the executive searches for the termination section, if one exists, and executes it. The executive then reads records until an end-of-file is read. It is important to note here for batch systems that the ODS system is not capable of slewing through test data cards that might be in the card reader between test sections. The only possible way to move data cards through the card reader is to select the test section that reads data cards. This limitation is most obvious with the card reader test, which has a large number of data cards. These data cards may be inserted into the card reader between the overlay decks; but any attempt to cause the executive to slew through the data cards causes problems.

If the system load device is the card reader, this imposes limitations on the operation of the overlay system. The card reader cannot be rewound. The following example illustrates the problem:

A test consists of four overlays; each overlay contains two sections (see figure 2-1). The following section selections are made: 1, 2, 3, 4, 1, 5, 8. All functions well until section 4 has completed. Section 1 does exist but it is in overlay 1. Overlay 2 is currently in the machine, so the executive is not able to find section 1. It reads overlays 3 and 4 and the end-of-file in a futile attempt to find section 1. It then writes a section not found message on the CDT and attempts to find the next selected section, which is section 5. This section is not found either because it is in overlay 3 and overlay 4 is currently in the machine. Since an end-of-file has already been

TABLE 2-2. LEVEL II LOADING PROCEDURES

Procedure	Method/Command	Comments/Messages
Manual Interrupt	<ol style="list-style-type: none"> 1. Press the CNTRL and BELL buttons simultaneously. 	The message MI is issued.
Load Only	<ol style="list-style-type: none"> 1. Type in: ODS, LOAD, tstnm 2. Press RETURN key on the console keyboard. 	<p>Loads and suspends the test specified by tstnm (test name). If the specified test is not found, an error message is issued. (Refer to level II test sections for further information and error messages.) When the test is loaded the following message is issued:</p> <p style="padding-left: 40px;">tstnm SUSPEND LOAD</p> <p>As many tests as memory allows can be loaded by repeating the LOAD command. ODS error message 11 is issued if core has been exceeded. For 8K systems no multiplexing of tests is allowed, thus only one test may be loaded and executed at a time. (See the Overlays Structure section for further information.)</p>
Load and Execute	<ol style="list-style-type: none"> 1. Type in: ODS, LDGO, tstnm 2. Press the RETURN key on the console keyboard 	The load and go command is only used when no parameter changes are desired. This command loads and executes the test specified by tstnm (test name).
Execute the Test	<ol style="list-style-type: none"> 1. Type in: ODS, GO, tstnm 2. Press the RETURN key on the console keyboard 	Starts execution of suspended test specified by tstnm (test name).
	<ol style="list-style-type: none"> 1. Type in: ODS, GO 2. Press the RETURN key on the console keyboard 	Starts execution of all suspended tests

found, no attempt is made to read more overlays to find section 5, and another section not found message is issued. Section 8 is found because it is in the last overlay (overlay 4), which is currently in the machine.

The overlay structure was designed to accommodate the 8K macro memory operation requirement placed on the ODS system. Therefore, multiplexing is not supported in the overlay version of the level II tests.

Level II diagnostics come in two versions; an overlay and a non-overlay version. The overlay version runs under an ODS overlay monitor and does not support multiplexing. The non-overlay version runs under an ODS multiplex monitor and does not support overlays, but allows for the repetition of any test.

The above description of the overlay operation is provided to allow the operator to make intelligent section selections if he changes the test default section selections.

Table 2-3 supplies the overlay breakdown for each ODS diagnostic test.

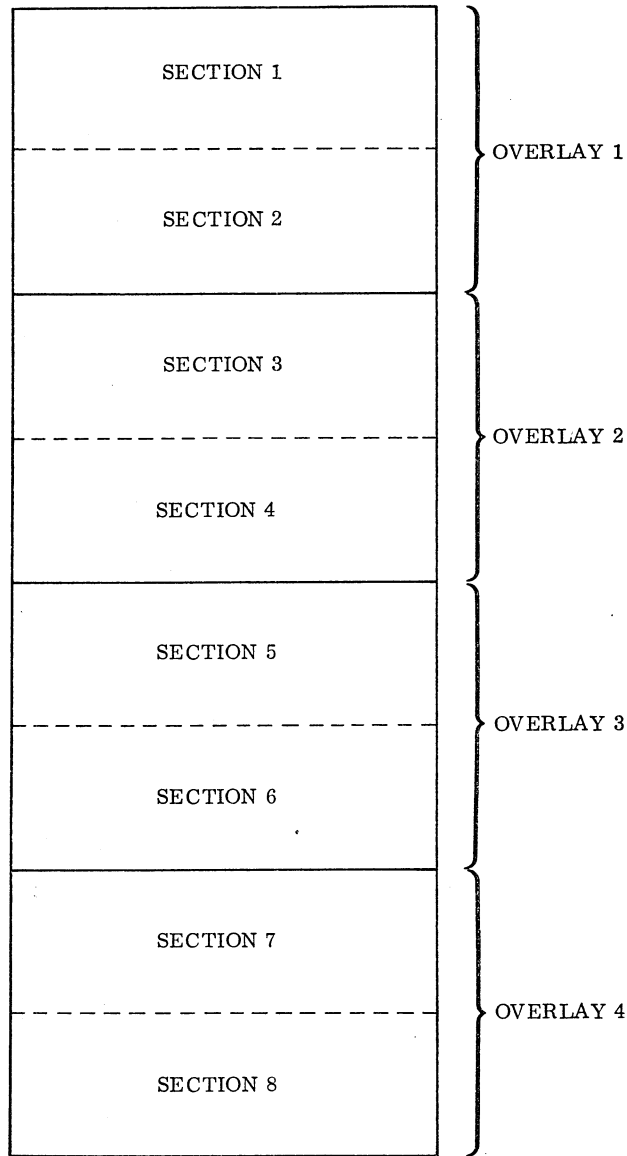
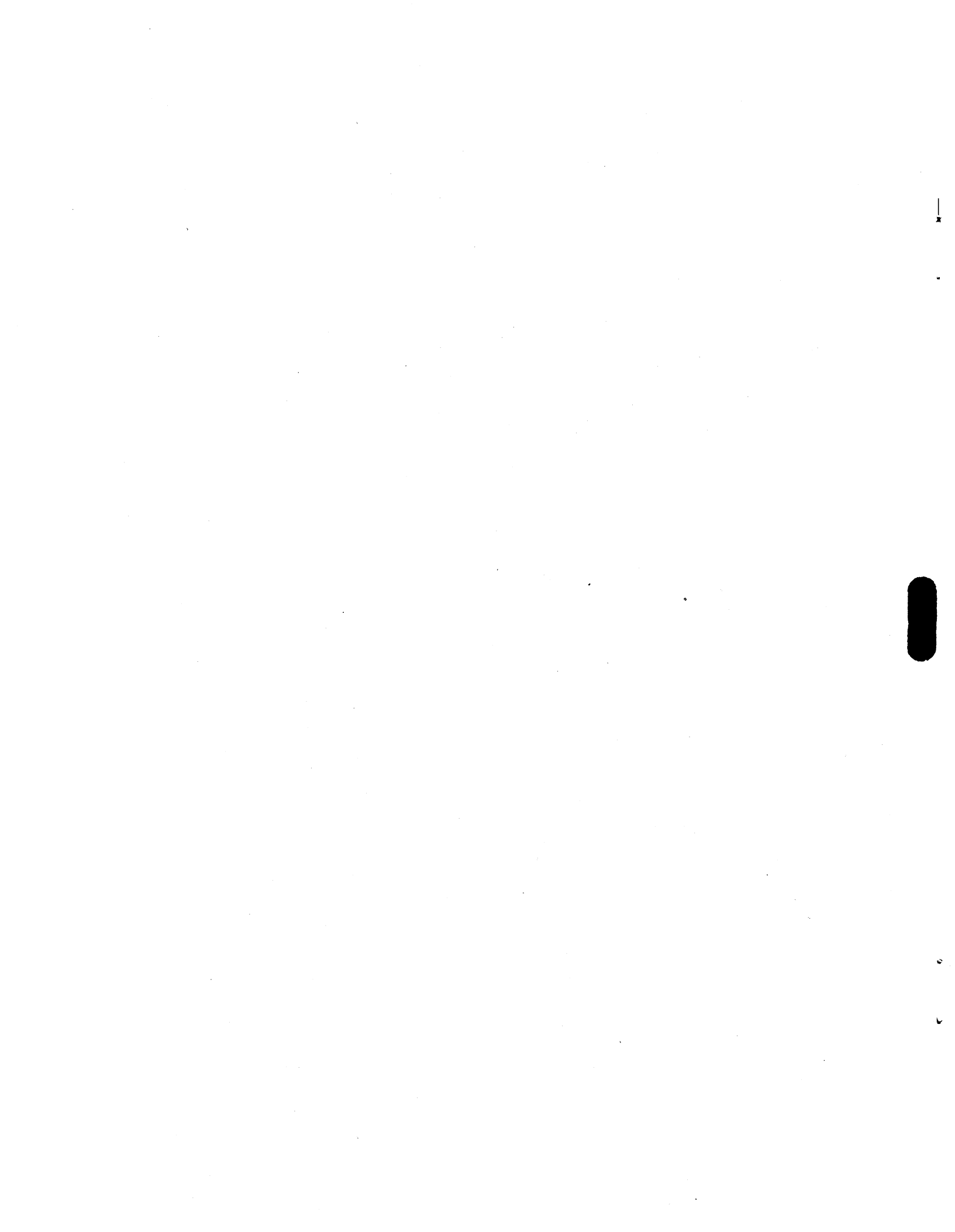


Figure 2-1. Overlay and Section Selection Example

TABLE 2-3. DIAGNOSTIC TEST OVERLAY STRUCTURE

Test Name	Overlay Version		Level
	Overlay	Section (Hex)†	
MPINS	1	0, 1, 2, 3, 4	I
	2	5, 6, 7, 8, 9	
MPMEM	1	0	I
	2	1	
	3	2	
	4	3	
	5	4	
	6	5, 10	
MPRTC	1	0, 1, 2, 3, 4, 5, 10	I
LIAT2	1	0, 1, 2, 3, 4, 5	I
		6, 7, 8, 9	
CRECO	1	0, 1, 2, 3, 4, 10	I
CR104	1	0, 1, 2, 3	II
	2	4, 5	
LP408	1	0, 1, 2, 3, 4,	II
	2	5, 6, 7	
CRUT1	1	0, 1, 2	II
CRUT2	1	0, 1	II
LCTTA	1	0, 1, 2, 10	II
LCTTB	1	0, 1	II
	2	2	
	3	3	
	4	4	
	5	5	
	6	6	
	7	7	
	8	8	
	9	9, A, B, C, 10	
CLA2A	1	0, 1, 2	II
	2	3	
	3	4	
	4	5, 6	
	5	7	
	6	8	
	7	9	
	8	A	
	9	B	

†Section 0 is the initialization section.
Section 10 is the termination section.



Each ODS diagnostic test consists of a maximum of 11_{16} sections:

- Section 0 is the initialization section
- Sections 1 through F are the diagnostic sections
- Section 10 is the termination section

All tests have an initialization section but not necessarily a termination section. All tests have at least one diagnostic test section. Each diagnostic test section may contain 0 through 4095 subsections.

The initialization section is executed before any diagnostic section when the test is first put into execution. It is executed again whenever the test is restarted (not to be confused with repeated).

The termination section is executed after the last selected diagnostic section has completed. It is also executed just prior to the initialization section if the test has been restarted. The abort function also causes the termination section to be executed.

The operator can select or bypass the initialization section or the termination section of an ODS diagnostic test only by aborting or restarting the test. A test is restarted by the ODS executive if the operator changes the section selections after the test begins execution. The restart occurs after entering the first GO function following a change in section selection words.

OPERATOR CONTROL OF TESTS

The operator can exercise a large amount of control over the execution of the diagnostic tests. The operator may select sections to be executed in any order (for restrictions, see the Overlay Structure section), request halts at various logical points during the test execution, and request that subsections, sections, and even the entire test be repeated. In addition to controlling logical flow of the diagnostic test, the operator may alter a number of parameters specific to a particular diagnostic test.

RUN PARAMETER CONTROL

Test control is realized through individual sets of run parameters. Each test has a maximum of 24 words of run parameters and a minimum of 12 words. The run parameters are used to control the execution and messages of each test program. The first 12 words of the parameter list contain standard parameters used by each test. The remaining 12 words of the parameter list contain optional parameters used for special functions.

Each test's run parameters may be displayed and, with the exception of TESTID, PASCNT, and ERRCNT, may be modified only when the test is suspended. The test control word, however, is modified with the CCW command even if the test is executing.

Figure 3-1 illustrates the run parameter list format. A description of each word and its bits is given in table 3-1.

SECTION SELECTION

Each diagnostic test consists of a number of operator selectable sections. The parameter list of a test contains four section selection words. Each four-bit hexadecimal digit represents a section. Up to 16 sections (1 through F_{16}) may be selected. A zero terminates section selection. The test initialization and termination sections are non-selectable. The initialization section executes whenever a test has to initialize counters and pointers. All selected sections are executed the number of times specified.

A test terminating section, if one exists, is then executed by the monitor at the completion of all specified passes for that test. The termination section performs the necessary clean up and housekeeping tasks that may be required at the completion of a test (but not at the completion of each pass).

After a test section completes, it is reported to the monitor. The monitor either transfers control to the

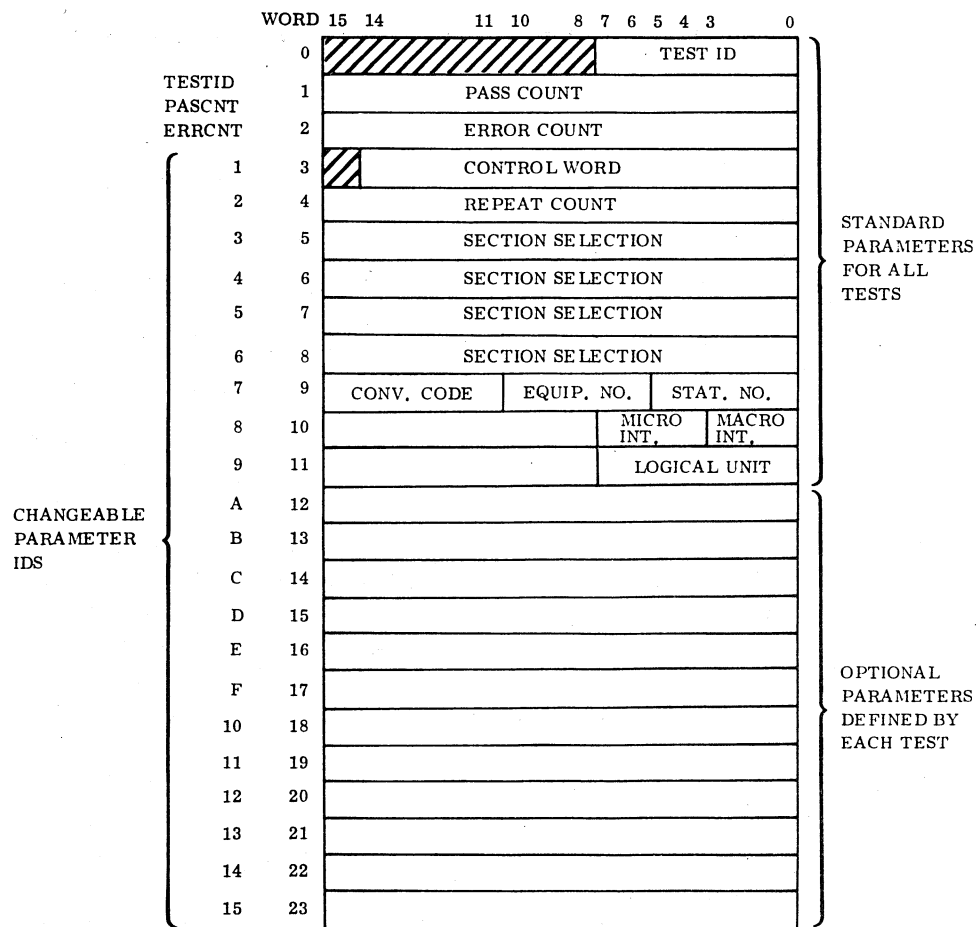


Figure 3-1. Run Parameter List

next selected section, if any, or to the same section if the repeat-section flag in the control word is set.

TEST REPETITION

When the last selected section of a test reports to the monitor that it is completed, one pass is considered complete for that test. The monitor then increments the test pass count. If the pass count has reached the specified repetition on count for the test, the test is terminated unless the repeat-test flag in the test control word is set. In this case, the pass count is allowed to exceed the specified repetition count. When repeating a test, the initialization and termination sections are not executed.

SECTION REPETITION

Each diagnostic test is composed of a number of repeatable sections. Each section uses a monitor subroutine (ENDSEC) to control its repetition according to the repeat section bit in the test control word. In addition, the subroutine determines whether or not the test is to be suspended at the end of the section.

SUBSECTION REPETITION

Each diagnostic test section is composed of a number of repeatable but not selectable subsections. Each subsection uses a monitor function (RPTSSC) to control its repetition according to the repeat-subsection bit in

TABLE 3-1. RUN PARAMETER DESCRIPTION

Run Parameter ID	Bits	Description
TESTID	15 through 8 7 through 0	Reserved for system expansion Two hexadecimal digits designating the test identification code. The digits are the leftmost digits of any action code issued by the diagnostic tests.
PASCNT	15 through 0	Four hexadecimal digits designating the number of passes (times the test has executed). The pass count is incremented by one every time a pass is completed. It is reset to zero whenever a test is restarted.
ERRCNT	15 through 0	Four hexadecimal digits designating the detected error count of the test executing. The error count is reset to zero whenever a test is restarted.
01	15 through 0	See figure 3-2 for a bit-by-bit description of the control word.
02	15 through 0	Four hexadecimal digits designating the number of times a test is to be repeated. When the pass count equals the test repeat count, the test is terminated. If the repeat test bit is set (bit 10 of the control word), the repeat count is overridden. The maximum value is 7FFF.
03-06	15 through 0	Each hexadecimal digit in the four words going from left to right selects a test section to be executed. These four words describe to the ODS executive the order in which the diagnostic sections are to be run. Each hexadecimal digit is the section number of a section of the diagnostic the operator wishes to execute. Diagnostic test sections execute in the order they are selected by the section selection words reading from left to right starting with the first selection word. The ODS executive continues to execute the test sections until all selected sections have been executed or a zero byte is extracted from the selection words. (See restrictions on section selection in the Overlay Structure section.) If a section selection is changed by the operator after the test has begun execution, the test is restarted.
07	15 through 11 10 through 7 6 through 0	Converter code of peripheral — Zero if not applicable Equipment number of peripheral Station number — Zero if not applicable
08	15 through 8 7 through 4 3 through 0	Reserved for system expansion Micro-interrupt line number of peripheral — Zero if not applicable Macro interrupt line number of peripheral — Zero if not applicable
09	15 through 8 7 through 0	Reserved for system expansion Logical unit number — Zero if not applicable
A-15	—	Optional run parameters defined by each test. Refer to test descriptions for parameter definitions.

the test control word. In addition, this function determines whether or not the test is to be suspended if an error has been detected in that subsection.

MULTIPLEXING

Multiplexing is the mechanism of transferring control to the various tests in core so that the processor's time is divided among those tests. This division is accomplished by specifying that a diagnostic test relinquish control to the monitor as soon as it gains control at its I/O request continuation addresses. The monitor then schedules the next test in core that is ready to be scheduled. By using this scheme, no test is allowed to waste processor time by looping waiting for I/O completion while other tests are waiting to initiate their I/O. This scheme approximates an operating system as much as possible. No other mode of multiplexing is employed by ODS. Overlay systems are not capable of multiplexing.

ABORTING OF TESTS

A level I test is aborted by master clearing the processor.

When it becomes necessary to abort a level II running test without halting the processor or the system, the following command may be entered after a manual interrupt:

ODS, ABRT, tstnm (cr)

Where: tstnm is the name of the test to be halted.

This causes the specified test to be halted at the end of either the subsection or section currently executing and the termination section (if one exists) to be executed. If the test name is omitted, every executing test is terminated. In order to restart an aborted test, the test must be reloaded.

RESTARTING A TEST

To restart a level I test, the P register must be reset to 0.

When a level II test is restarted via the ODS, RSTR, tstnm command, execution is suspended at the end of the next subsection or section, whichever comes first. The

termination section (if it exists) is executed, and then the initialization section is executed. The selected test sections are then executed as directed by the section selection words in the test parameter list.

SKIP SWITCH CONTROL

In addition to the control exercised through the parameter list, the operator can cause the tests to halt at every possible stop by setting the skip switch on the micro processor. See section 4 (System Operator Communication) for the format of setting the skip switch.

MASTER CONTROL WORD

In addition to the control exercised through the parameter list and the skip switch, the system supports a master control word. The master control word has the same format as the test control word (see figure 3-2). Setting bits in the master control word affects all tests in the system, whereas setting a bit in the test control word affects only that test. Whenever the system needs to look at the control word, it does an inclusive OR of the master control word and the test control word.

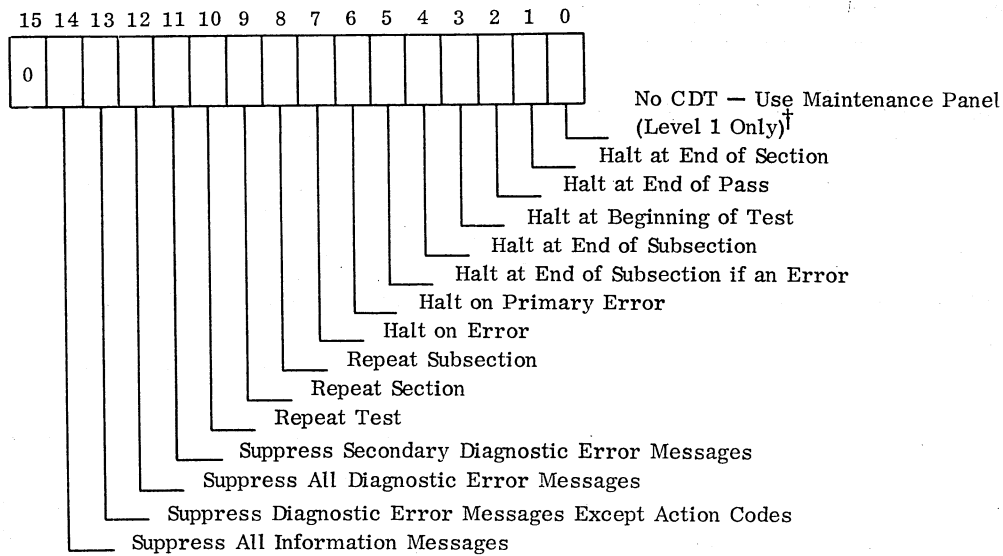
Figure 3-2 illustrates the test control word of the run parameter list. Table 3-2 is a description of each of the bits and their functions.

PARAMETER DISPLAY AND ENTRY FOR LEVEL I TESTS

The method of parameter display is based on setting bit 0 of the control word; 0 is set for program mode display and 1 is set for panel interface mode.

For level I tests, the run parameters may be displayed by pressing the RETURN key on the console keyboard or changed any time the test is suspended. Figure 3-3 shows the format of the parameter display.

If the no CDT bit is set in either the test control word or the master control word, control is never passed to the run parameter display software, and as a result the machine does not halt with the run parameter message number in the A register. Inspection and modification of a test's run parameters are possible when the machine halts with a suspension message number in the A register; at this time the Q register contains the address of the tests run parameters.



† If this bit is set, no attempt is made to read or write from the system comment device. When the system needs to write a message to the operator, the system macro halts and the operator should inspect the A register to determine the message number.

Figure 3-2. Control Word

TABLE 3-2. DESCRIPTION OF CONTROL WORD OF BITS AND THEIR FUNCTIONS

Bits	Description
15	Zero
14	Suppress all informative messages.
13	Suppress diagnostic error messages except action code. If this bit is set, only the action code portion of an error message is output.
12	Suppress all diagnostic error messages. If this bit is set, no diagnostic error messages are output to the CDT.
11	Suppress secondary diagnostic error messages.
10	Repeat test. If this bit is set, the test is repeated and the pass count is incremented until the bit is cleared.
9	Repeat section. If this bit is set, the active section is repeated until the bit is cleared.
8	Repeat subsection. If this bit is set, the system repeats the active subsection of a test section until the bit is cleared.
7	Halt on error. If this bit is set, the test is suspended when a diagnostic error is detected.
6	Halt at primary error. If this bit is set, the test is suspended only after a primary error.
5	Halt at end of a subsection if there is an error. If this bit is set, the test is suspended at the end of the subsection that detected the error.

TABLE 3-2. DESCRIPTION OF CONTROL WORD OF BITS AND THEIR FUNCTIONS (Continued)

Bits	Description
4	Halt at end of a subsection. If this bit is set, the test is suspended at the end of each subsection execution.
3	Halt at beginning of test flag. If this bit is set, the test is suspended at the beginning of the test and outputs an information message.
2	Halt at end of pass. If this bit is set, the test is suspended when it completes a pass.
1	Halt at end of section flag. If this bit is set, the test is suspended at the end of a section.
0	No CDT (level I only) flag. If this bit is set, the system does not use a CDT.

tstnm RUN PARAMETERS

```

TEST ID  PASCNT  ERRCNT  0001  0002  0003  0004  0005
xxxx    xxxx    xxxx    xxxx  xxxx  xxxx  xxxx  xxxx

0006    0007    0008    0009  000A  000B  000C  000D
xxxx    xxxx    xxxx    xxxx  xxxx  xxxx  xxxx  xxxx

000E    000F    0010    0011  0012  0013  0014  0015
xxxx    xxxx    xxxx    xxxx  xxxx  xxxx  xxxx  xxxx
    
```

RUN PARAMETER MODIFICATION

See the System Operator Communication section (section 4) for the parameter modification commands and procedures.

Where: tstnm is the test name
 xxxx is the hexadecimal value of a parameter
 0001 is the control word
 0002 is the repeat count
 0003-0006 is the section selection
 0007 is the equipment code
 0008 is the interrupt lines
 0009 is the logical unit
 000A-0015 are defined by each test if used

Figure 3-3. Parameter Display

This section describes the special keys, commands, and special functions that the operator can use to control execution, modify tests, terminate tests, and certain functions related to diagnosing errors. (For further information on error diagnosis and further special functions, refer to the ODS Messages and System Malfunctions section (section 5) and the hardware maintenance manual.

SPECIAL KEYS

The following keys on the CDT and the optional BOP have specific functions for use in the ODS system.

SLASH (/)

The slash (/) is used for input error corrections made from the keyboard. It can be used to correct any field where an error has been made, except for the ODS portion of level II commands. A field is whatever appears between the commas of a command. When an error is caught in a field, the operator simply types a slash (/) and re-enters the correct field values. If an error occurred in an earlier field, the RUBOUT/LINE FEED and (cr) must be used for error correction.

Examples:

5, 148¢/1486

ODS, LOAD/LOAD, TEST A

The / is valid for both level I and level II commands with the exception that the first field of all level II commands is the word ODS.

RUBOUT/LINE FEED

The RUBOUT and LINE FEED keys followed by a carriage return are used for correcting whole lines or any error that cannot be handled by the slash (/).

Example:

ODS, LAOD, CR104 Entered from the keyboard

To correct, press RUBOUT/LINE FEED (cr) and re-enter the correct entry of the command

ODS, LOAD, CR104

CARRIAGE RETURN

The carriage return key ((cr)) is used to send commands to the system.

CNTRL/ BELL

The CNTRL and BELL keys are pressed simultaneously to cause a manual interrupt for level II commands. If successful, the level II monitor displays an MI on the CDT or types it out on the TTY.

BOP SPECIAL KEYS

The BOP (optional on some systems) keys and lights are described below.

RUN

The RUN key is used for system macro go. The RUN key also has a light that indicates when lit that the system is running and when not light that a macro halt has occurred.

MASTER CLEAR

The MASTER CLEAR key is used for deadstarting the system.

AUTOLOAD

The AUTOLOAD key is used for starting the card reader (deadstarting) to read cards.

LEVEL I COMMANDS

Level I of ODS supports five types of commands. They are:

- Skip switch
- Deadstart parameters
- GO
- Change parameters
- Display parameters

SKIP SWITCH

The skip switch is not a physical switch that can be toggled, but a bit that can be set by the operator. Setting the skip switch during level I operation causes the system to halt at all possible system halts. The skip switch must be turned off before loading the level II monitor.

The possible halts caused by setting the skip switch are:

- Halt at end of section
- Halt at end of pass
- Halt at beginning of test
- Halt at end of subsection
- Halt at end of subsection if errors
- Halt on primary error
- Halt on error

The procedure for setting the skip switch is:

1. Press the ESCAPE key.
2. Type in J26@.

The procedure for turning the skip switch off is:

1. Press the ESCAPE key.
2. Type in J22@.

DEADSTART PARAMETERS

The user can customize the LODCHK deck to fit the particular installation requirements by changing the deadstart parameters. See the LODCHK section (section 6) for the description of the deck and parameters.

GO

When any level I test is suspended, the operator can cause the test to continue or start execution by entering the command

GO (cr)

The GO command is also used to terminate parameter entry when changing test parameters.

CHANGE LEVEL I PARAMETERS

When a level I test is suspended, the operator may change the test's run parameters. Parameters are changed by typing in the index of the first word to be changed followed by the new data values to be stored into successive parameter locations. The input string is terminated with either a carriage return (cr) or a GO (cr). The input of any illegal values results in the re-issue of the parameter list. Up to 36 characters including blanks may be entered. All parameters except the TESTID, PASCNT, and ERRCNT can be changed or modified. The format for parameter modification is as follows:

h, qqqq, qqqq, qqqq, qqqq, qqqq, qqqq, qqqq (cr)

Where: h is a one-digit hexadecimal number indicating the index value of the first word of the parameter list to be changed.

qqqq is a one- to four-digit hexadecimal number indicating the data value(s) to be stored into the parameter list.

The following are two examples of parameter modification:

1. If section selection word 3 had data values of 1234 and section selection word 4 had data values of 5678 and the operator wished to modify the parameters to execute only sections 1, 3, 5, 7, and 8,

he would enter the following after the test was suspended:

3, 1357, 8000 (cr)

2. If the operator wished to change run parameters that were not in contiguous locations, two separate entries would be made or, if quicker, the parameter words in between would be repeated. For example, if the control word (run parameter 1) had hexadecimal value 80 and the operator wanted to change it to 2080 and also change the section selection words as in example 1, the changes would be entered in one of two ways. First the operator could make two separate entries:

1, 2080 (cr)

3, 1357, 8000 (cr)

or he could change the parameters by including the existing value of run parameter 2 (assume a value of 0002), thus making only one entry:

1, 2080, 0002, 1357, 8000 (cr)

If the parameter entry is valid, no message is issued. Further, if the section selection parameter words (3 through 6) are selected, the test is restarted. Otherwise the test resumes execution from the point of suspension. (See the Overlay Structure section for certain overlay version restrictions on section selection and restarting of tests.)

DISPLAY PARAMETERS

When the test is suspended, any input by the operator other than a GO or a legal change parameter input causes the test parameters to be displayed or typed out. Typically, the user can cause parameters to be displayed by typing a carriage return. For the format of the parameter display see figure 3-2.

When a test is suspended at the beginning of the test, end of section, or end of pass, it can be restarted by setting the P register to 0000. Restart can also be accomplished by changing the section selection words in the test's run parameter list (see the Run Parameter Modification section — section 3).

LEVEL II COMMANDS

Level II ODS has two types of commands that the operator can use to affect the system. The first command is to set the skip switch. When the operator sets the skip switch, the system automatically suspends each of the tests when the test comes to a place where a stop may have taken place if the control words had been set to stop there.

NOTE

It is important that the operator should not leave the skip switch set while loading a test into the machine.

The second type of command for level II is controlled by interrupting the system. When the operator enters a manual interrupt (CNTRL/BELL keys), the system responds with MI and awaits a command to be input by the operator. There may be a slight delay before MI is typed out. If there has been no response after about five seconds, the operator should try again. Once the system has responded with an MI message, all the diagnostics in execution have stopped and do not start again until the input is completed.

The complete format of each level II command is given below. It is absolutely necessary to enter the ODS portion of the command starting at column 1 with no embedded blanks following it. If the ODS portion of the command is entered incorrectly, the system responds with the following message:

MI INPUT ERROR

In order to correct the error, the operator must do a manual interrupt and re-enter the command correctly.

LOAD

Whenever the operator wishes to load a new diagnostic test into the system, he can use the LOAD command (see also LDGO). The format for this command is:

ODS, LOAD, tstnm (cr)

Where: tstnm is the name of the test to be loaded.

If the specified test is already in the system, an executive error message is generated. If the test cannot be found, one of two things can happen:

1. In the level II overlay version, the processor is halted because the card reader has run out of cards. At this point there are two possible things to do — If the test whose name is specified in the command does not exist, the operator must start the level II system over again, starting with LODCHK. If the test does exist, the correct decks must be found and placed into the card reader.
2. In a level II non-overlay system, the system issues the following message:

L, 10 FAILED xx ssss

to which the operator may respond with either an RP to continue looking for the specified test or a CU to stop the reading. If the CU is the option selected, then there is no more system activity with regard to the test.

When a test is found, it is loaded and immediately suspended and this message is issued:

tstnm SUSPENDED LOAD

Where: tstnm is the test name.

DISPLAY PARAMETERS (DPAR)

Once a test has been loaded into the machine, the operator may need to look at the parameters currently being used by the test. The DPAR command is used for that purpose. The format is:

ODS, DPAR, tstnm (cr)

Where: tstnm is the test name.

If the specified test is not currently in the machine, an executive error message is generated. If the test is found, the parameters are displayed or typed out according to the format described in the Run Parameter section (section 3).

CHANGE PARAMETERS (CPAR)

If the operator wants to change the parameters for a specific test, then the CPAR command is used. The format for this is:

ODS, CPAR, tstnm, x, yyyy, yyyy, yyyy, ... (cr)

Where: tstnm is the test name.

- x is the number of the first parameter to be changed. 1 is the control word and 15₁₆ is the last word in the parameter list.
- y is the data value to be put into the parameter list starting at entry x. There can be from one to four data values entered.

All of the numbers are to be entered in hexadecimal and only the first four characters are used. The system issues an error message if the specified test is currently running. If the CPAR request is accepted by the system, then there is no response. If the section selection words are changed, the test is restarted when a GO function is entered.

DISPLAY CONTROL WORD (DCW)

If the only parameter that the operator wants to display is the control word, then the operator should use the DCW command. The format for DCW is:

ODS, DCW, tstnm (cr)

Where: tstnm is the name of the test or the word MASTER (for the master control word).

If the system cannot find the specified test, an error is generated. When the control word is displayed, it comes out in the following form:

tstnm CONTROL WORD = xxxx

Where: tstnm is the name of the test.

xxxx is the hexadecimal value of the specified control word.

CHANGE CONTROL WORD (CCW)

If the only parameter that the operator wants to change is the control word, the operator should use the CCW command. The format of CCW is:

ODS, CCW, tstnm, xxxx (cr)

Where: tstnm is the name of the test or the word MASTER (for the master control word).

xxxx is the new control word value to be entered.

If the system cannot find the specified test or the new control word value is illegal, an error is generated. If the test name is found and the control word value is valid, then there is no reaction from the system. This command can be used to modify a test's control word while the test is running.

GO

Whenever a test has been suspended for any reason, it is necessary to tell the system to start the test running again. The GO command is used to do this. Its format is:

ODS, GO, tstnm (cr)

ODS, GO (cr)

Where: tstnm is the name of the test that the operator wants to start executing or continue executing.

If no name is specified (second command format), then all suspended tests in the system are started. (See the Overlay Structure section in section 2 for 8K level II restrictions.) If the specified test is not in the system (first format) or there are no suspended tests in the system (second format), an error message is generated.

RESTART (RSTR)

Whenever the operator wishes to start a diagnostic test over from the beginning, he should use the RSTR command. The format of RSTR is:

ODS, RSTR, tstnm (cr)

ODS, RSTR (cr)

Where: tstnm is the name of the test that the operator wants to restart.

If no name is specified (second format), then all the tests in the system are restarted. If the specified test is not in the system (first format), or there are no tests in the system (second format), an error is generated. When a test is restarted, both the termination and initialization sections are run unless the test's initialization section has not yet been run. Therefore, in the case of any level II test with overlays, the RSTR command should be used with caution (see the Overlay Structure section in section 2).

ABORT (ABRT)

If the operator wishes to stop the execution of a diagnostic and remove it from the system, the ABRT command is used. The format of ABRT is:

ODS, ABRT, tstnm (cr)

ODS, ABRT (cr)

Where: tstnm is the name of the test that the operator wants to abort.

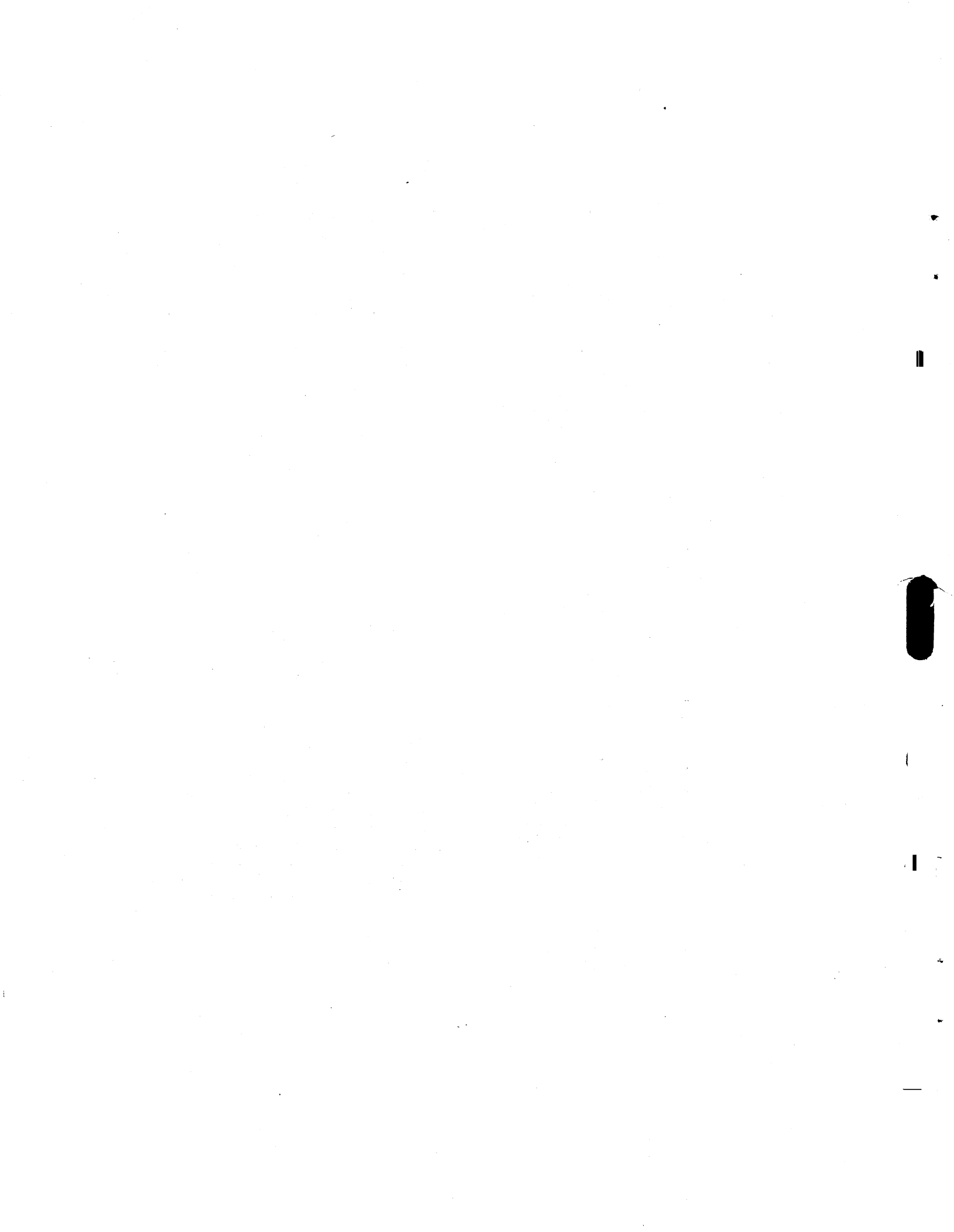
If no name is specified (second format), then all of the tests in the system are aborted. If the specified test is not found (first format) or there are no tests in the system, an error is generated.

LOAD AND GO (LDGO)

The LDGO command combines the operation of the LOAD command and the GO command except for the fact that the test is immediately started (not immediately suspended). The format and error detection is identical to the LOAD command. This command is used whenever the preset parameters of the diagnostic test are acceptable to the operator. The LDGO command can be very helpful in speeding up operation of the system. The format of LDGO is

ODS, LDGO, tstnm (cr)

Where: tstnm is the name of the test.



The ODS system reports a large number of messages to the operator. These messages are provided so the operator can make decisions based on what the system discovered.

MESSAGE NUMBERS

All ODS messages except monitor messages and LODCHK messages have a two-digit hexadecimal message number associated with them. The actual messages, along with their message numbers (if applicable), are listed in table 5-1. The message number is used as follows:

1. During level I operation, if the system or test is running without a CDT (see description of the control word) for use in program mode, the processor macro halts when a message is available for the operator. The operator uses the maintenance panel to look at registers and memory as required by the particular message. The A register should contain the code

ttmm

Where: tt is the test ID (zero for a system message not initiated by the test)
mm is the message number.

The Q register contains the address of an additional block of data in main memory specific to the message number (if Q register is zero, no additional data exists for this message).

The operator may continue execution by issuing a macro go, after being sure the P register, if changed, is reset to its value at the time the macro halt occurred. The operator may restart the test by setting the P register to 0000 and issuing a macro go.

2. In the event that a fatal error is detected by the system, the processor macro halts with the A register containing

00mm

Where: mm is the message number.

The Q register should be zero.

MESSAGE CATEGORIES

There are eight categories of messages reported by the ODS system. They are:

- Fatal errors
- Executive error messages
- Suspension messages
- Diagnostic errors
- Informative messages
- Action messages
- LODCHK messages
- Monitor messages

Not all messages result in output of information; some result in a macro halt condition. In the case of the optional basic operators panel (BOP), it causes the RUN light to go out.

FATAL ERRORS

A fatal error requires that the ODS system come to an immediate halt, with the A register containing

00mm

Where: mm is the message number.

The first digit of the message number should be 0 or 1. The Q register should be zero. (Refer to table 5-1 for messages and actions to be taken.)

EXECUTIVE ERROR MESSAGES

An executive error message is displayed on the CDT when the ODS monitor detects an operator input error. The first digit of an executive error message should be 2. If the system is running with the no CDT bit set in the master control word and the A register is 0021₁₆ when the machine stops, the Q register should contain the address of a core location. This core location contains the ASCII code for the type of ODS error that has been detected.

TABLE 5-1. ODS MESSAGES

Test	Message	Message No.	Definition/Action†
All level II tests	None	04	Many unrequested interrupts occurred on an interrupt line to which the system thinks a device is currently connected. System assumes constant interrupt. Correct and reload system.
All level II tests	None	05	More scheduled calls were made and not completed than the scheduler could handle. Reload system using back-up deck. If error persists call the on-site analyst.
All level I tests	None	07	Interrupt occurred on interrupt line whose mask register is zero. Interrupt should not have occurred. Reload system.
All level I tests	None	08	Unexpected protect fault interrupt occurred. Reload system.
All level I tests	None	09	Unexpected parity fault interrupt occurred. Reload system.
All level I tests	None	0A	CDT error detected on input. Repeat input operation by giving micro processor a macro go.
All level I tests	None	0B	CDT error detected on output. Repeat output operation by giving micro processor a macro go.
All level II tests	None	0C	Some test parameter list contains logical unit number that is out of range of system. Reload and check logical units in parameter lists of tests running at time of failure.
All level I-II overlay tests	None	0D††	Ready and not busy status did not occur on card reader within allowable time. Reload system.
All overlay tests	None	0E	Data status did not occur within allowable time on card reader. Reload system.
All overlay tests	None	0F	End of Operation status did not occur within allowable time (no alarm occurred). Reload system.
All overlay tests	None	10	Card reader not ready before reading first card of deck. Ready card reader and issue macro go.
All overlay tests	None	11	Card reader alarm status occurred for conditions other than empty hopper or full stacker. Reload system.
All overlay tests	None	12	Card deck sequence error. Reload system using new deck.

†A cross reference to the diagnostic decision logic tables (DDLTs) in the hardware maintenance manual should be made for complete corrective action for all messages requiring operator intervention.

††Message numbers OD-1C are card reader errors detected by the loader while loading diagnostic overlays (other than the first overlay) or EOF cards in level I or while loading all overlays for level II.

TABLE 5-1. ODS MESSAGES (Continued)

Test	Message	Message No.	Definition/Action
All overlay tests	None	13	Record input from card reader is too large for available memory. Reload system.
All overlay tests	None	14	Card deck checksum error. Reload system.
All overlay tests	None	15	Card reader external reject — director status 2. Reload system.
All overlay tests	None	16	Card reader internal reject — director status 2. Reload system.
All overlay tests	None	17	Card reader external reject — director status 1. Reload system.
All overlay tests	None	18	Card reader internal reject — director status 1. Reload system.
All overlay tests	None	19	Card reader external reject — data input. Reload system.
All overlay tests	None	1A	Card reader internal reject — data input. Reload system.
All overlay tests	None	1B	Card reader external reject — feed function. Reload system.
All overlay tests	None	1C	Card reader internal reject — feed function. Reload system.
All level II tests (non-overlay)	L, 10 FAILED xx ssss ssss = Last hardware status xx = Equipment malfunction code 00 Interrupt timeout 01 Lost data 02 Alarm error (read check, stacker full, etc.) 04 Checksum error 05 Internal reject 06 External reject 09 Sequence error 10 Non-negative record length 12 No 7/9 punch in column 1 14 Device not ready 34 Data interrupt after 80 columns 35 Early EOP interrupt	None	Card reader failure occurred during loading. Type CU (cr) in response to the message ACTION. Put deck back in card reader and request load again.
All level II tests	MI	5A	Manual interrupt (CNTRL and BELL) has been received and system is waiting for ODS level II command.

TABLE 5-1. ODS MESSAGES (Continued)

Test	Message	Message No.	Definition/Action		
All level II tests	MI INPUT ERROR	26	Command did not begin with ODS. Re-enter command.		
All tests	tstnm COMPLETED xxxx PASSES	52	Test specified by tstnm has completed xxxx passes for the selected sections. No action required.		
All tests	tstnm EXECUTING	50	Test specified is currently executing. No action required.		
All tests	tstnm SUSPENDED xxxx xxxx = SELF ERR BOT ENDS ENDP LOAD SUBE SUBH	30	Test specified has suspended itself.		
		31	Diagnostic detected error and the halt on error control word bit was selected.		
		32	Diagnostic suspended at beginning of specified test.		
		33	Current section of specified test has finished and halt at end of section bit control word was selected.		
		34	All selected sections have been executed for specified test and halt at end of pass bit in control word was set.		
		35	Specified test was successfully loaded and suspended following LOAD command.		
		36	Specified test has been suspended at end of current subsection after an error was diagnosed.		
		37	Specified test has been suspended after finishing current subsection.		
					For messages 30 through 37, operator may change parameters at this point, if desired, and then enter ODS, GO, tstnm to continue.
		All tests	All ODS diagnostic messages	40	Check the action code by getting the address of the error packet from the Q register.
All tests	tstnm SECTION xxxx	51	Section specified by xxxx for tstnm has started execution.		
All tests	tstnm RUN PARAMETERS...	55	Diagnostic run parameters for test specified are displayed.		
All tests	tstnm TERMINATED xxxx ERRORS	53	Diagnostic test specified has been terminated with xxxx errors during execution.		
All level II tests	ODS BUSY	28	ODS is currently busy processing last command entered. Re-enter command.		
All level II tests	ODS ERROR xx xx = 01 Invalid command mnemonic 02 Third field must be entered 03 Test not available 04 Command not valid for master parameter list	21	Operator command input error occurred during loading of test or while test was not processing. Re-enter the command correctly.		

TABLE 5-1. ODS MESSAGES (Continued)

Test	Message	Message No.	Definition/Action
	05 Too many field inputs for command		
	06 Non-hexadecimal input		
	07 Invalid parameter		
	08 Invalid parameter index		
	09 Test not currently suspended		
	10 No change parameter data input		
	11 Test being loaded is too large for available core.		
All level II tests	OV	N/A	Overflow of monitor's volatile core has occurred. Reload system.
All level II tests	PE	N/A	Macro core parity fault interrupt has occurred. Reload system.
All level II tests	PF	N/A	Protect fault interrupt has occurred. Reload system.
All level II tests	PW	N/A	Power failure interrupt has occurred. Reload system.
All tests	tstnm SECT xxxx NOT FOUND	22	Section xxxx selected for tstnm could not be found at time it was to be run. Reload test and run proper sections in correct sequence.
MPINS	MULTILEVEL INDIRECT SWITCH IS EXPECTED TO BE OFF	54	Multilevel indirect switch parameter A is zero.
MPINS	MULTILEVEL INDIRECT SWITCH IS EXPECTED TO BE ON	54	Multilevel indirect switch parameter A is non-zero.
MPMEM	ADDRESSING ERROR IN STACK xx	54	Contents of stack or interstack addresses did not match, total number of stacks specified is different from value computed, or start and/or stop address specified is wrong.
MPRTC	CLEAR PROTECT AND STOP SWITCHES (ESC J20 @ GO CR)	72	
MPRTC	SET PROTECT AND CLEAR STOP SWITCHES (ESC J28 @ GO CR)	73	
MPRTC	SET PROTECT AND STOP SWITCHES (ESC J2A @ GO CR)	71	
MPRTC	VERIFY THE CPU IS HALTED AT xxxx (ESC J11: K:) AND RESTART CPU (I@)	70	xxxx = Address of where processor should be stopped. Compare value for K with value in message; then press I@.
MPRTC	CLEAR PROTECT AND SET STOP SWITCHES (ESC J22 @ GO CR)	61	

TABLE 5-1. ODS MESSAGES (Continued)

Test	Message	Message No.	Definition/Action
LIAT	LAMP CHECK	N/A	Verify that the KEYBOARD LOCK, CHAR, CO, and CTS lights stay on for about 30 seconds. Optional indicators RTS, DTR, TRANS DATA, and REC DATA (if present) should also be verified.
LIAT	ENTER 1234567890 FROM KEYBOARD	N/A	
LIAT	ENTER UP TO 80 ALPHANUMERIC CHARACTERS INCLUDING (cr)	N/A	If less than 80 characters are entered, (cr) must be pressed.
LIAT	WITHIN 30 SECONDS DO THIS INPUT "LOCK" HIT BREAK KEY INPUT "UNLOCKED"	N/A	
LIAT	WITHIN 30 SECONDS DO THIS SWITCH TO ODD PARITY INPUT ONE ALPHANUMERIC CHARACTER SWITCH TO EVEN PARITY INPUT ONE ALPHANUMERIC CHARACTER	N/A	
LIAT	A/Q pattern ADT CHAR pattern ADT WORD pattern	N/A	Visually judge data transmission of each pattern.
CRECO	CR IS DISABLED	54	Card reader is disabled on the board.
CRECO	LP IS DISABLED	54	Line printer is disabled on the board.
CR104	MAKE CARD READER READY WITHIN 30 SECONDS	N/A	Place card decks into card reader and press RESET button on device.
CR104	MAKE CARD READER NOT READY WITHIN 30 SECONDS	N/A	Empty card hopper or press STACKER FULL switch.
CR104	MAKE THE INPUT HOPPER EMPTY AND STACKER FULL WITHIN 30 SECONDS	N/A	Lift the card deck in input hopper and simultaneously press stacker switch.
CR104	MAKE THE INPUT HOPPER NOT EMPTY AND STACKER NOT FULL WITHIN 30 SECONDS.	N/A	Press the RESET button.
CR104 CRUT1 CRUT2	ROW NO. 12 11 0 1 2 3 4 5 6 7 8 9 TOTAL ERROR COL	N/A	Message given for every column of a card with an error. Where blank equals no error, 1 equals column not punched but read as being punched, 0 equals column punched but read as being not punched.
CR104 CRUT1 CRUT2	n GHOST INTERRUPTS OCCURRED	N/A	Appears at end of each section where a ghost interrupt occurred. MI ODS, GO, CR104 (cr)

TABLE 5-1. ODS MESSAGES (Continued)

Test	Message	Message No.	Definition/Action
CRUT1	LOAD SYNC ADJUSTMENT DECK	N/A	Separate test data deck that must be loaded. MI ODS, GO, CRUT1 (cr)
CRUT1	LOAD READ ADJUSTMENT DECK	N/A	Separate test deck that must be loaded. Perform these actions: MI ODS, GO, CRUT1 (cr) Row and error information for above message also appears for this message.
CRUT2	WAITING UNTIL MOTOR TIMES OUT	N/A	No action is required.
CRUT2	1. DELAY TO FIRST CARD COLUMN FROM A FEED REQUEST A. FEED MOTOR OFF B. FEED MOTOR ON 2. DATA RATES AFTER FIRST COLUMN 3. CARD CYCLE TIME 4. CARD RATES CPM	MIN xxxMS .xxMS xxxMS xxx	MAX AVG xxxMS xxxMS .xxMS xxxMS xxx
LP408	PRESS STOP ON LINE PRINTER	N/A	Press STOP button on line printer cabinet.
LP408	PRESS START ON LINE PRINTER WITHIN 30 SECONDS	N/A	Press START button on line printer cabinet.
LCTTB	REMOVE WRITE RING AND MAKE UNIT READY WITHIN 180 SECONDS	N/A	Press UNLOAD button, remove write ring, press LOAD button and then press READY button.
LCTTB	INSERT WRITE RING AND MAKE UNIT READY WITHIN 180 SECONDS	N/A	Press UNLOAD button, insert write ring, press LOAD button and then press READY button.
CLA2A	PROTECT BIT (ON)	N/A	Informative message only
CLA2A	PROTECT BIT (OFF)	N/A	Informative message only
CLA2A	LOOK AT BOP 0	N/A	Informative message only
CLA2A	LOOK AT BOP 1	N/A	Informative message only
CLA2A	CLA BOARD BAD	N/A	Replace board and rerun test.
CLA21	ASYNC BAUD RATE CHAN xy x = 0 or 1 y = 19.2, 9600, 4800, 2400, 1200, 600, 300, or 110	N/A	Informative message only

SUSPENSION MESSAGES

A suspension message is displayed on the CDT whenever a diagnostic test is suspended from execution. The operator must issue a GO command to cause the test to continue execution following test suspension. The first digit of the suspension message should be 3.

If the system is running with the no CDT bit set in the master control word or the test control word, the system stops with the address of the run parameter list in the Q register. The operator may inspect and modify the run parameter via the maintenance panel interface. Changing the section selection words via the panel interface does not cause the test to restart, as it does when those words are changed using the level I or level II commands via the CDT.

DIAGNOSTIC ERRORS

Diagnostic errors are detected by ODS diagnostic test programs. When a test detects an error it issues an error message containing the following information:

1. The test name
2. English text briefly describing the error
3. An action code
4. The number of the test section and the number of the subsection within the test section that detected the error
5. The number of passes through all selected sections before the present error was detected
6. The equipment code
7. The micro and macro interrupt line numbers
8. A number of hexadecimal words that contain error data peculiar to this action message (optional)

A diagnostic error message is displayed in its entirety, suppressed completely, or suppressed except for the test name and action code. These options are selectable by setting bits in either the test control word or the master control word. The format of the diagnostic error message is:

```
Line 1  tstnm English-text
Line 2  CODE=xxee, SECT=sxxx, PASS=pppp,
        ERR0=cccc, EQCD=qqqq, ILNS=00ij
```

Where: tstnm is the five-character name of the test.

English-text is the explanation of the test error (maximum of 16 characters).

CODE is the action code.
 xx = ID of test detecting the error
 ee = Error code.† (First digit of error code is standardized for specific error conditions.)
 1e = Reject on input function
 2e = Reject on output function
 3e = Status error
 4e = Data error
 5e = Interrupt error
 6e = Protect fault
 7e = Parity error
 Error codes greater than 7 are unique to the test generating the code.

SECT is the section number.
 s = Section
 xxx = Subsection

PASS is the pass count (pppp)

ERR0 is the error count (cccc)

EQCD is the equipment code and station (qqqq)

ILNS is micro and macro interrupt line numbers
 i = Micro interrupt line number
 j = Macro interrupt line number

Additional lines of data may be printed depending on the action code. The specific mnemonics and four-digit hexadecimal data values in additional lines are defined in the individual test sections of this manual.

The action code supplied in the diagnostic error message is a hexadecimal four-digit number that leads the operator to an entry in the diagnostic decision logic table (DDLTL). It is composed of two parts. The left-most two digits are the identification of the test that detected the error and issued the diagnostic error message. The right-most two digits are the error code originated by the running test. Thus the action code is always unique, since the test identification is unique.

†Except for LODCHK and MPINS

The third digit of the action code is standardized so identification is always by the same digit regardless of what peripheral is being tested. The contents of the A and Q registers for the different types of messages is shown in table 5-2.

When the A register contains a diagnostic message code, the Q register contains the address of an error packet in macro memory.

The format of that error packet is shown in figure 5-1.

The operator must look at this error packet in macro memory via the maintenance panel to determine the action code and other data pertaining to this error. Words 8 through n are the additional data values peculiar to the action message.

The operator may continue execution by issuing a macro go, after being sure the P register (if changed) is reset to its value at the time the macro halt occurred. The

TABLE 5-2. A AND Q REGISTER CONTENTS FOR ALL MESSAGE TYPES

Message Type	A Register†	Q Register
Fatal	000x 001x	0000
Executive	002x	If not zero, the address of a memory location containing the ODS error code in ASCII
Suspension	tt3x	Address of test run parameter list
Diagnostic	tt4x	Address of error packet
Informative	tt5x	0000
Action	tt6x through ttFx	0000

†The last two digits of the A register are the message numbers and are used to index the message table.

††tt = test ID. 0 if message originated from ODS executive.

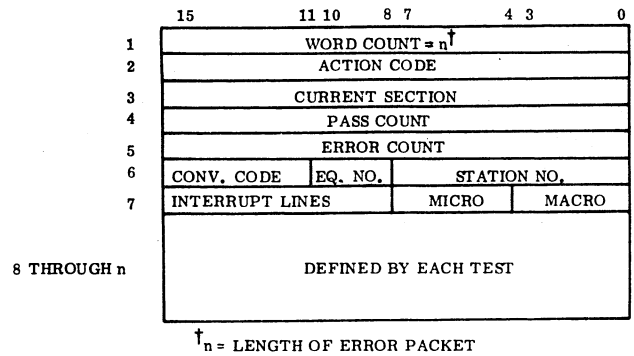


Figure 5-1. Diagnostic Error Packet

operator may restart the test by setting the P register to 0000 and issuing a macro go.

INFORMATIVE MESSAGES

An informative message is issued by the ODS system to inform the operator of the state of the diagnostic test. The first digit of the message type is 5.

ACTION MESSAGES

An action message is an English text message issued by the diagnostic test. This message instructs the operator to do something. The first digit of the message type is 6 through F.

LODCHK MESSAGES

The LODCHK program is always the first program of the ODS system to be loaded into the main memory of the micro processor. It makes initial checks of instructions, memory, and the load path. These checks are primitive and assume that little of the micro processor is functioning. As such, its messages are primitive; selective stops with the value in the P register indicating the error that was detected. The P register, rather than the A or Q registers, is used to indicate an error. If the test executes at all, the A register and the Q register could be failing, but at least the P register would be working.

LODCHK also contains a loader used to load level I diagnostics and the level II monitor. This loader also uses selective stops with the P-register value indicating the type of error. Additionally, LODCHK writes the digits 1, 2, 3, 4, 5, and 6 to the CDT to indicate that certain sections of LODCHK have completed. For a complete description of LODCHK and its errors and messages, see the Loadcheck section (section 6).

MONITOR ERROR MESSAGES

Monitor error messages are output by the system as a result of a system failure. The system failures include failure of the load device, the mainframe, or the software. There is no association made with message numbers.

MESSAGE FORMATS

The text and meaning of messages issued by the ODS system is described in alphabetical order in table 5-1. Fatal errors have no actual text listed and appear in message number order. Some messages, such as LODCHK, monitor, and level II messages have no message number associated with them; in these cases N/A appears in the message number column.

For the messages with message numbers, the first digit of the message number is the type of message. The message numbers and their meanings are:

0x	= Fatal
1x	= Fatal
2x	= Executive error
3x	= Suspension
4x	= Diagnostic error
5x	= Informative
6x through Fx	= Action

DETECTING SYSTEM MALFUNCTION

This section is to be used as a guide for detecting system malfunctions. (See the hardware reference manual for displaying and modifying registers.) If the machine is macro halted, compare the value of the P register with the values listed in LODCHK for action code stops. If there is a match, LODCHK has detected an error

and has halted the machine. If there is no match, compare the lower 8 bits of the A register with the message numbers in table 5-1. Note that if the A register matches a code other than one of the fatal codes, the system (or test) is running without a CDT for use in program mode. Check to see if the test or master control word has the no CDT bit set. The no CDT bit only applies to level I. If the lower 8 bits of the A register cannot be found in table 5-1, the machine has stopped for an unexplained reason.

If the machine is not macro halted, be sure that the CDT is not in panel mode. If it is in panel mode, the ODS software may be waiting to display a message on the screen. Put the CDT in program mode to allow pending messages to be displayed. If a message is displayed, look the message up in table 5-1 or check to see if one of the following messages has been displayed:

- PW — Power failure
- PE — Parity error
- PF — Protect fault
- OV — Overflow volatile storage

If one of these was issued as the last output, look up the message in table 5-1. If no message was printed, see if the P register is 0000 and the X register is 18FF. If they are, this indicates a power failure detected in level I. If not, the error is unknown.

If a system failure is detected, do the following:

1. Bring the machine to a macro halt.
2. Copy down the contents of the following registers:
 - P
 - A
 - Q
 - I
 - M
 - FCR
3. Dump core if possible — Refer to Memory Dump (appendix H) for the dump program.
4. Fill out a DPSR form completely describing what events led to the failure.

Figure 5-2 is a flowchart describing briefly the procedure discussed in this section.

SYSTEM PATCHING

If a system malfunction occurs that requires a fix as a result of a DPSR, a system patch with detailed instruc-

tions on installing the patch will be TWXed or a complete binary deck sent.

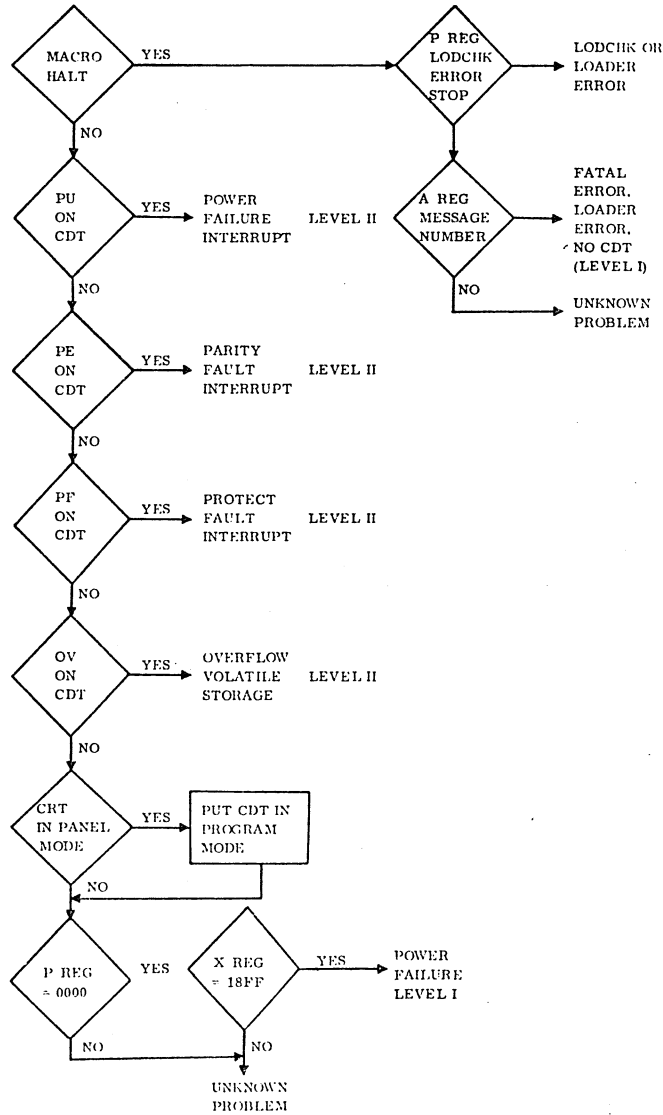
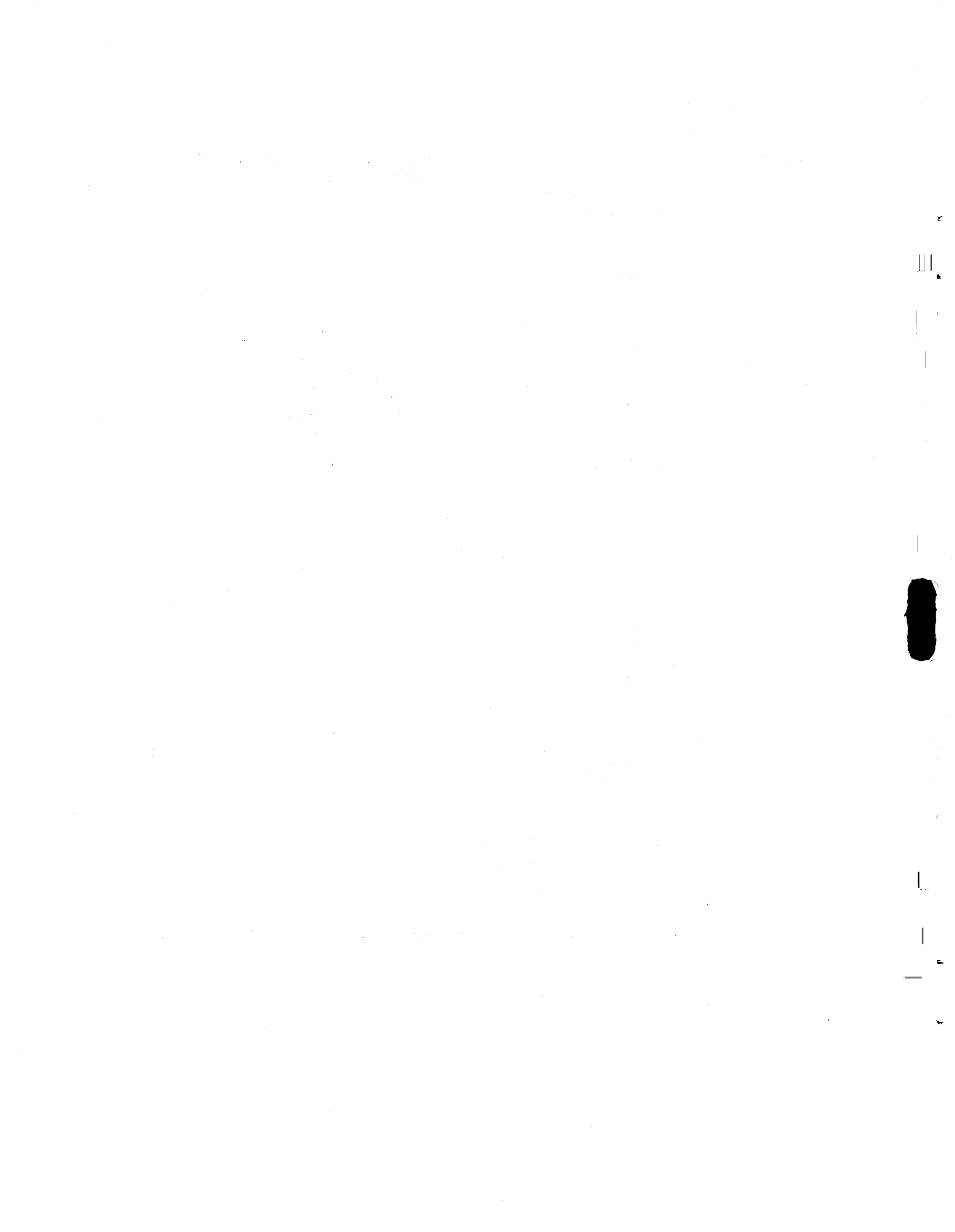


Figure 5-2. Procedure for Detecting System Malfunctions Using CDT



PURPOSE

LODCHK verifies the load path required for stand-alone diagnostics after LODCHK performs a checksum function to determine it has been loaded properly. The load path is defined as all the hardware components required to load a binary object program. The instructions used by the loading process, the core storage used, and to a limited extent the load device, are all checked. Instructions that are used by the checksum function are tested beforehand.

After the load path has been tested, the next program in the load device is loaded starting at location zero. At the end of the program load, the loader transfers control to location zero.

The completion of each LODCHK section is noted by a number appearing on the CDT. A 123456 indicates successful execution of the six LODCHK sections. All hardware malfunctions detected are noted by action codes presented as P register values.

LODCHK FLOW

LODCHK is the first program loaded into the processor. It is loaded at location 1000_{16} using the deadstart feature of the processor. The LODCHK deck consists of a diagnostic, a loader, a set of parameters, and a set of cards used to check the A/Q load path between the card reader and the processor. Deadstart loads all the cards in the deck except the cards used to check the A/Q load path. Figure 6-1 illustrates the typical system flow for LODCHK, level I tests, and the level II monitor.

The diagnostic portion of LODCHK makes a quick check of memory, instructions, the CDT, and the load path. It then moves the loader and the parameters to the high part of stack zero. The address of the loader is stored in location $1FFF_{16}$. After LODCHK is finished executing, the memory appears as illustrated in figure 6-2.

After moving the loader and parameters to the high part of stack zero, LODCHK transfers control to the loader. The loader immediately attempts to read data to load a program that it expects to be in the card reader. If the card reader hopper is empty, the loader executes

The loader immediately attempts to read data to load a program that it expects to be in the card reader. If the card reader hopper is empty, the loader executes a selective stop, which halts the machine at location $1EF6_{16}$. If the machine halts, the operator must put the desired card deck into the card reader input hopper and push the RESET button to make the device ready. Giving the processor a macro go causes it to load the deck in the card reader into memory starting at location 0.

After the loader has loaded the program, it transfers control to the program by jumping to location 0.

If the program is a level I diagnostic test, the executive, using the test ID as an index, moves the parameters for this test from the top part of stack zero (where they were stored by LODCHK) into the local test parameter list. The executive then passes control to the various test sections, as defined by parameters in the

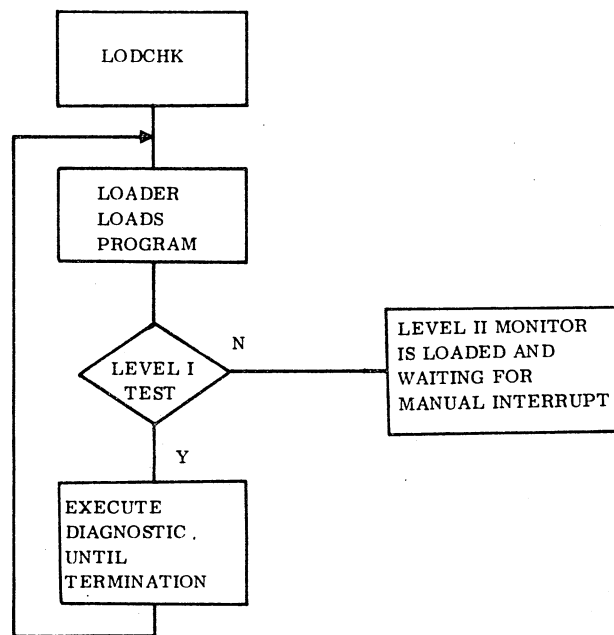


Figure 6-1. LODCHK System Flow

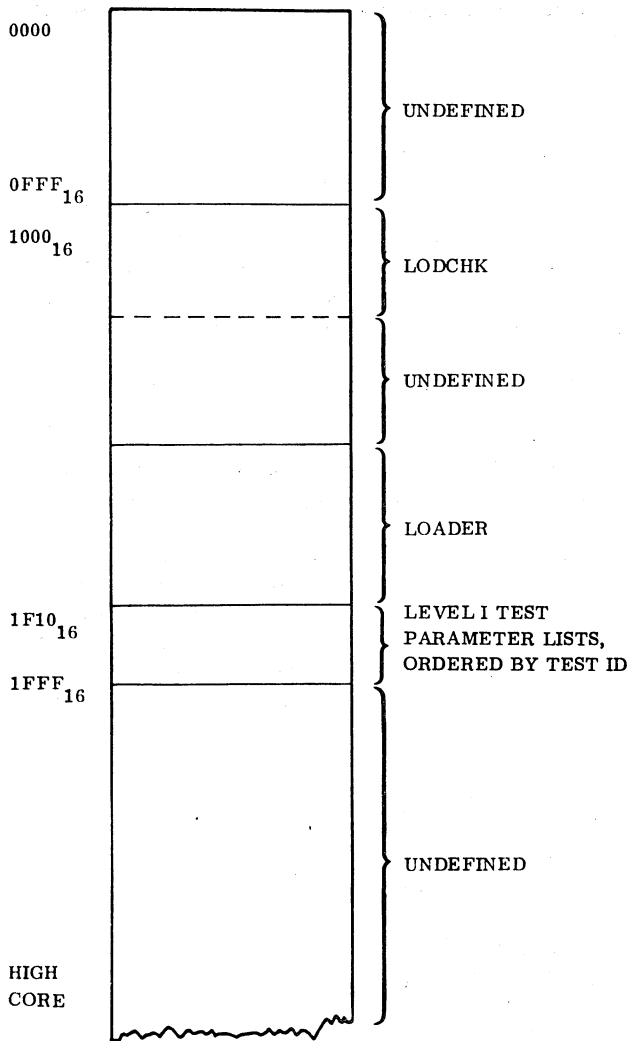


Figure 6-2. Memory Map After LODCHK Loading

local test parameter list. If the operator changes any of the parameters, it is important to note that the operator changes them only locally and does not change the parameters that LODCHK has stored in the high part of stack 0.

When the level I executive determines that the test has terminated execution, it transfers control to the loader by jumping to its first word address. The loader and the parameter lists are resident in main memory from the time LODCHK is deadstarted into the machine until the level II monitor is loaded by the loader.

If the program is the level II monitor it prints the message:

ODS x.xx

Where: x.xx is the system identification.

The level II monitor then activates the interrupt system and waits in the idle loop for a manual interrupt.

PARAMETERS

The parameters for all level I tests are deadstarted into the machine when LODCHK is deadstarted in. The last six cards in the LODCHK deck are a control card and five cards read by LODCHK to test the load path. The 30 cards preceding the last six contain the parameters for LODCHK itself and nine level I diagnostics (i.e., 24 words per test, eight words per card, three cards per test). The user may customize the parameters in the LODCHK deck to fit his particular installation. Figure 6-3 is a listing of the deadstart parameter cards.

The first number in each group, except for LODCHK, contains the test ID that is the first word of the parameter list for each test. Parameter 23 of LODCHK's parameter is used as the level I master control word.

LODCHK requires the equipment code of the load device. This indicates the load device that contains the test pattern records (required by the load path test) and the programs to be loaded.

The only parameter that may be modified is the equipment code of the load device. It is preset to the standard card reader. The parameter may be changed to the desired equipment code. See Level I Record Organization (appendix E). The equipment codes for each installation should be checked when the system is installed, as equipment codes may vary from site to site.

ORGANIZATION

LODCHK is organized into the following components:

1. Command test (part 1)
2. Checksum

	<u>TEST ID</u>	
0000G0000G0000G0000G0000G0000G0000G0000G0000G0000G	9	Test Name
0000G0000G0000G0000G0000G0000G0000G0000G0000G0000G		
0000G0000G0000G0000G0000G0000G0000G0000G0000G0000G		
0008G0000G0000G2080G0001G1234G0000G0000G0000G0000G	8	CRECO
0000G0580G0088G0000G0200G0044G0055G0001G		
0000G0000G0000G0000G0000G0000G0000G0000G0000G0000G		
0007G0000G0000G2082G0001G1234G5678G9000G	7	LIAT2
0000G0091G0011G0004G000C60000G0000G0000G0000G0000G		
0000G0000G0000G0000G0000G0000G0000G0000G0000G0000G		
0006G0000G0000G2080G0001G1234G5000G0000G	6	MPRTC
0000G00F3G0088G0000G1FFF60000G0000G0000G0000G		
0000G0000G0000G0000G0000G0000G0000G0000G0000G0000G		
0005G0000G0000G2080G0001G1234G5000G0000G	5	MPMEM
0000G0000G0000G0000G0000G0000G0000G0000G0000G0000G		
0001G0000G0000G0000G0000G0000G0000G0000G0000G0000G		
0000G0000G0000G0000G0000G0000G0000G0000G0000G0000G	4	
0000G0000G0000G0000G0000G0000G0000G0000G0000G0000G		
0000G0000G0000G0000G0000G0000G0000G0000G0000G0000G		
0000G0000G0000G0000G0000G0000G0000G0000G0000G0000G	3	
0000G0000G0000G0000G0000G0000G0000G0000G0000G0000G		
0000G0000G0000G0000G0000G0000G0000G0000G0000G0000G		
0000G0000G0000G0000G0000G0000G0000G0000G0000G0000G	2	
0000G0000G0000G0000G0000G0000G0000G0000G0000G0000G		
0001G0000G0000G2080G0001G1234G5678G9000G	1	MPINS
0000G0000G0000G0000G0000G0000G0000G0000G0000G0000G		
0000G0000G0000G0000G0000G0000G0000G0000G0000G0000G	0	LODCHK
4352G0008G0000G0000G0000G0000G0000G0000G0000G0000G		
0000G0000G0000G0000G0000G0000G0000G0000G0000G0000G		
0000G0000G0000G0000G0000G0000G0000G0000G0000G0000G		
K1000G 010G		Control Card
		K41202800+

Figure 6-3. Deadstart Parameter Cards

3. Command test (part 2)
4. Memory test
5. Load device test
6. Mover
7. Section completion noting
8. Loader
9. Parameter lists
10. Data for load path check

The following seven instructions are tested in the order presented:

1. LDA — Load A (two-word address)
2. INQ — Increase Q
3. LDQ — Load Q (two-word address)
4. CLR — Clear a register
5. SWN — Skip if skip switch is not set
6. SWS — Skip if skip switch is set
7. JMP — Jump (two-word address)

SECTION 1 — COMMAND TEST (PART 1)

Part 1 of the command test is the first routine to execute. Its function is to test the basic processor and emulator paths and to test the instructions required in the execution of the checksum.

The remaining repertoire (listed below) may be tested in any order. However, the testing of an instruction does not use any instruction not previously tested.

- ENA — Enter A
- INA — Increase A

- ENQ — Enter Q
- Drp — Decrement and repeat
- XFr† — Enhance instruction transfer to r
- JMP — Jump relative
- SUB — Subtract
- TRQ — Inter-register transfer to Q
- TRM — Transfer to M
- RAO — Replace add one in storage
- ALS — A left shift
- SCA — Store character from A
- ARA — Add memory to register A
- SEF — Set field to ones
- SFA — Store field from A
- SRG — Store registers
- LRG — Load registers
- ASC — Scale
- SFZ — Skip if field zero
- LCA — Load character to A
- MUI — Multiply integer
- DIV — Divide
- INP — Input to A

If the instructions do not function properly, an action code is reported in the P register. If the instructions do function properly, 1 is displayed on the CDT screen and LODCHK begins checksum operations.

SECTION 2 — CHECKSUM TEST

The purpose of checksum is to verify that LODCHK was loaded properly. The binary values of all the words in LODCHK except the run parameters are added together by the checksum module. The checksum for LODCHK was generated before LODCHK was punched in deadstart format by the deadstart generator program (see Deadstart Format (appendix C)). The value attained was complemented and placed in the last word of LODCHK. Thus, the sum should be zero. If it is not zero, an action code is reported in the P register. If the sum is zero, 2 is displayed on the CDT screen.

†r = 1, 2, 3, 4, A, Q, I, r

SECTION 3 — COMMAND TEST (PART 2)

The function of part 2 of the command test is to test those commands or instructions that are required in the execution of the subsequent tests and functions:

- Memory test
- Load path test
- Mover
- Section completion noting
- Loader

The instructions to be tested are:

- LDA Load A relative (one-word addressing)
- TRA Transfer A to another register
- LDQ Load Q relative (one-word addressing)
- RAO Replace-Add-One to Memory (one-word addressing)
- TCQ Transfer and complement Q to another register
- LDA () Load A relative, indirect
- STA () Store A relative, indirect
- LDQ () Load Q relative, indirect
- ADQ () Add to Q relative, indirect
- LLS Long left shift (A and Q shift)
- SUB Subtract relative
- STQ Store Q (two-word addressing)
- ADQ Add Q relative
- EOR ADD, I Exclusive OR relative, indexed
- JMP (), Q JMP indirect, indexed (two-word addressing)

These instructions are tested in the same manner they are used in the LODCHK program. Before the memory test executes, this section attempts to clear memory parity errors from 0 through 0FFF by loading and storing each word in memory. Upon successful completion, 3 is displayed on the CDT screen.

SECTION 4 — MEMORY TEST

This test validates the lower half of stack zero. Only location 0 to FFF₁₆ is tested. This ensures proper loading of level I programs into these locations. The test consists of a combination of addressing and worst case test patterns (see Main Memory Test, section 7, for specific patterns). If a memory location does not pass the test, an action code is reported in the P register. If a memory location is valid, 4 is displayed on the CDT screen.

the input device. If no errors occur, 6 is displayed on the CDT screen. The results are illustrated in figure 6-5.

SECTION 5 — LOAD DEVICE TEST

The actual load device is tested by reading in a test pattern from the device. The device is selected in the parameter list by specifying the equipment code. The card reader test pattern illustrated in figure 6-4 is compared to a like pattern in memory. If the load device fails or the pattern does not compare properly, an action code is reported in the P register. If the load device checks out and the pattern tests compare, 5 is displayed on the CDT screen.

SECTION COMPLETION (NOTEND)

The NOTEND subroutine writes (via an A/Q transfer) to the CDT the number of the section that has just completed.

INFORMATIVE MESSAGES

There are no informative messages.

SECTION 6 — MOVER

The mover module moves the loader and the parameter list to the top of stack 0 and then executes the loader to read the next level I test or the level II monitor from

RESTRICTIONS

LODCHK restrictions are as follows:

1. Equipment code 91₁₆ and interrupt line 1 must be used for the CDT.
2. The selective stop bit in FCR must be on; the SELECTIVE SKIP switch must be off.

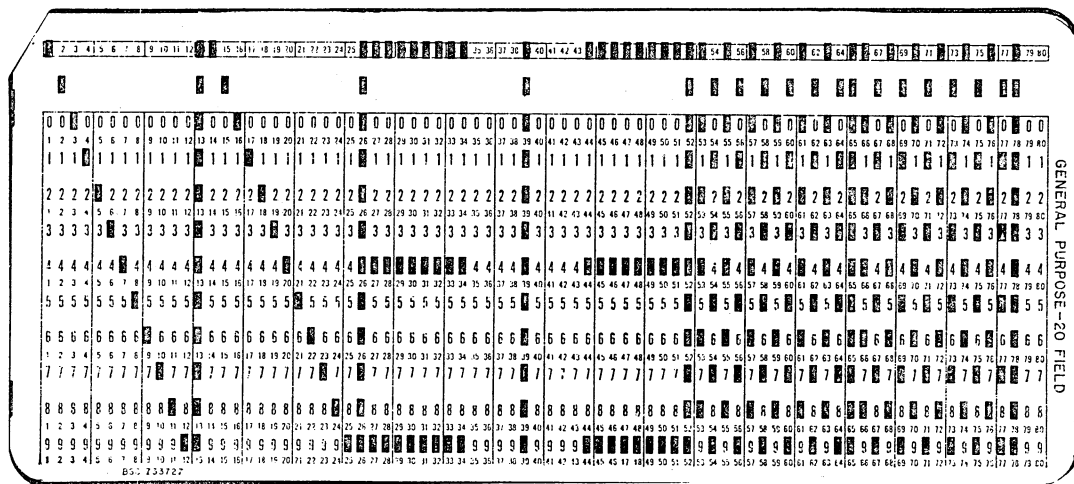


Figure 6-4. Load Test Pattern

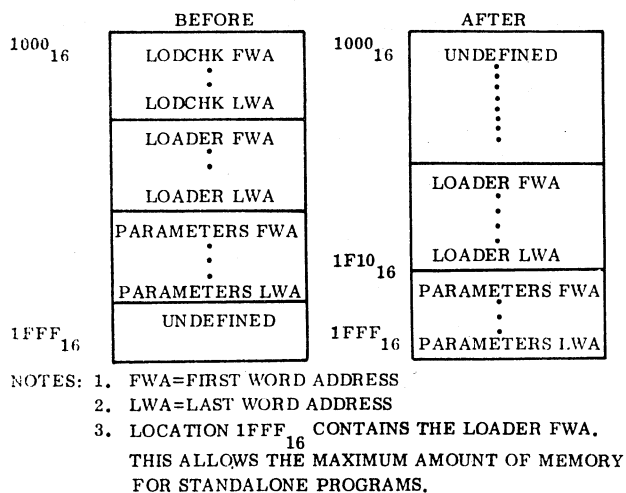


Figure 6-5. Mover Execution Results

If the load device fails, or a program checksum failure occurs, an action code is reported in the P register. Otherwise, control is passed to location 0, and the loader remains in core to load level I tests.

PARAMETER LISTS

Parameter lists for all stand-alone tests are initially loaded with LODCHK. Their integrity is maintained from one stand-alone test to another. This facilitates the execution of several stand-alone tests after executing LODCHK once. For a detailed description of the contents of the run parameter list entries, refer to figure 6-3 and to the specific sections as well as Level I Record Organization (appendix E).

ACTION CODES

The action codes of LODCHK and the LODCHK loader are presented in the processor's P register. When

LODCHK or the LODCHK loader halts, the operator must display the P register to observe the action code. Table 6-1 lists the LODCHK action codes.

It is assumed that LODCHK runs with the SELECTIVE STOP switch set, which causes the mainframe to halt (macro stop) when an error is detected.

If the halt was the result of a detected CDT error, giving the machine a macro go (I@) causes the program to continue ignoring the error.

If the halt was at $P = 108C_{16}$, an error has been detected in section 1 of LODCHK. Specifically, the error occurred during execution of one of the 26 instructions used to check basic paths through the emulator. Giving the machine a macro go carries the machine through a series of selective stops that enable it to determine precisely which of the 26 instructions is failing. To facilitate this process, the operator should refer to the program listing for LODCHK.

If the halt was not a $P = 108C_{16}$, pressing the RUN button causes the failing code to execute again. If the failure occurs again, the halt also occurs again. If the halt does not occur, the program continues with the next test. The operator might find advantage in troubleshooting by turning the SELECTIVE STOP switch off after detecting an error, and giving the machine a macro go. This causes the machine to execute the failing code over and over at high speed, assuming an error keeps occurring.

NOTE

If the error was associated with the load path test or the loader, giving the machine a macro go causes it to repeat the entire load path test or the entire load. This means that the operator must reload the cards into the input hopper before giving the machine a macro go.

TABLE 6-1. LODCHK ACTION CODES

Action Codes	LODCHK Error Definitions
P = 1003	LDA (2 WORD) FAILURE
P = 1006	INQ FAILURE
P = 1009	LDQ (2 WORD) FAILURE
P = 100C	CLR FAILURE
P = 100F	INTERNAL REJECT-DIRECTOR FN-INLINE CDT
P = 1011	EXTERNAL REJECT-DIRECTOR FN-INLINE CDT
P = 1013	INTERNAL REJECT-DATA-INLINE CDT
P = 1015	EXTERNAL REJECT-DATA-INLINE CDT
P = 1017	LODCHK CHECK-SUM ERROR
P = 101A	DATA TIMEOUT-SUBROUTINE CDT
P = 101C	INTERNAL REJECT-STATUS-SUBROUTINE CDT
P = 101E	EXTERNAL REJECT-STATUS-SUBROUTINE CDT
P = 1020	INTERNAL REJECT-DIRECTOR FN-SUBROUTINE CDT
P = 1022	EXTERNAL REJECT-DIRECT FN-SUBROUTINE CDT
P = 1024	INTERNAL REJECT-DATA-SUBROUTINE CDT
P = 1026	EXTERNAL REJECT-DATA-SUBROUTINE CDT
P = 1029	LDA* FAILURE
P = 102C	TRA FAILURE
P = 102F	LDQ* FAILURE
P = 1032	RAQ* FAILURE
P = 1035	TCQ FAILURE
P = 1038	LDA* () FAILURE
P = 103B	STA* () FAILURE
P = 103E	LDQ* () FAILURE
P = 1041	ADQ* () FAILURE
P = 1044	LLS FAILURE
P = 1047	SUB* FAILURE
P = 104A	STQ* FAILURE
P = 104D	STQ (2 WORD) FAILURE
P = 1050	ADQ* FAILURE
P = 1053	EOR* FAILURE
P = 1056	MEMORY PARITY ERROR
P = 1059	MEMORY ADDRESSING ERROR
P = 105C	MEMORY WORST CASE ERROR

TABLE 6-1. LODCHK ACTION CODES (Continued)

Action Codes	LODCHK Error Definitions
P = 105F	ILLEGAL DEVICE IDENT. CODE (IDC)
P = 1062	CARD READER TIMEOUT FOR EOP
P = 1064	INTERNAL REJECT CARD READER
P = 1066	EXTERNAL REJECT CARD READER
P = 1068	CARD READER DROPPED READY
P = 106A	INTERNAL REJECT CARD READER — OUTPUT
P = 106C	EXTERNAL REJECT CARD READER — OUTPUT
P = 106E	CARD READER TIMEOUT FOR DATA/BUSY
P = 1071	DATA READ FOR LOAD PATH CHECK WAS IN ERROR
P = 1073	SWN FAILURE
P = 1076	SWS FAILURE
P = 1079	AND* FAILURE
P = 107C	DQP FAILURE
P = 107F	ADD LABEL, Q FAILURE
P = 1082	STA LABEL, Q FAILURE
P = 1085	RTJ LABEL (2-WORD RELATED) FAILURE
P = 1088	JMP* () FAILURE
P = 108C	AN ERROR WAS DETECTED IN ONE OF THE 26 INSTRUCTIONS USED TO TEST THE BASIC EMULATOR PATHS DURING SECTION 1 EXECUTION OF LODCHK
P = 10D8	STOP FOR JMP FAILURE
P = 10DA	STOP FOR JMP* FAILURE
P = 1EF0	TIMEOUT WHILE WAITING FOR READY AND NOT BUSY STATUS BEFORE FEEDING A CARD
P = 1EF2	TIMEOUT WHILE WAITING FOR DATA STATUS WHILE READING ONE OF THE 80 COLUMNS OF DATA FROM A CARD
P = 1EF4	TIMEOUT WHILE WAITING FOR END OF OPERATION STATUS AFTER READING 80 COLUMNS OF DATA FROM A CARD
P = 1EF6	TIMEOUT WHILE WAITING FOR READY AND NOT BUSY STATUS BEFORE FEEDING FIRST CARD OF DECK
P = 1EF8	ALARM AT END OF OPERATION. ALARM NOT CAUSED BY HOPPER EMPTY OR STACKER FULL
P = 1EFA	SEQUENCE ERROR. LAST CARD READ WAS OUT OF SEQUENCE. FIRST CARD OF A DECK MUST HAVE SEQUENCE NUMBER 0000
P = 1EFC	RECORD (DECK) LAST READ WAS TOO LARGE TO FIT IN AVAILABLE MEMORY

TABLE 6-1. LODCHK ACTION CODES (Continued)

Action Codes	LODCHK Error Definitions
P = 1EFE	CHECKSUM ERROR. CHECKSUM FOR LAST RECORD (DECK) READ WAS NOT ZERO.
P = 1F00	EXTERNAL REJECT, DIRECTOR STATUS 2 INPUT
P = 1F02	INTERNAL REJECT, DIRECTOR STATUS 2 INPUT
P = 1F04	EXTERNAL REJECT, DIRECTOR STATUS 1 INPUT
P = 1F06	INTERNAL REJECT, DIRECTOR STATUS 1 INPUT
P = 1F08	EXTERNAL REJECT DATA INPUT
P = 1F0A	INTERNAL REJECT, DATA INPUT
P = 1F0C	EXTERNAL REJECT, FEED FUNCTION
P = 1F0E	INTERNAL REJECT, FEED FUNCTION

LODCHK2

LODCHK2 is the multiplex version of LODCHK. It is designed to operate with the multiplex ODS monitor and tests. LODCHK and LDCHK2 are functionally equivalent and are composed of the same basic parts. The differences between the two programs can be summarized as follows:

- LDCHK2 moves itself to the lower 4K portion of stack 0 to test all available memory, while LODCHK tests only the first 4K words of stack 0.
- The action codes for LDCHK2 are identical to those defined for LODCHK before LDCHK2 moves itself; that is, for the instruction test parts 1 and 2, the checksum and the lower memory test. After LDCHK2 moves itself to the lower portion of stack 0, the action codes correspond to those of LODCHK except for the left-most digit, which may have any value from 0 to 7. This digit indicates where LDCHK2 is executing when the error occurred. Zero means the first half of stack 0, 1 the upper half, 2 the lower half of stack 1, and so on.
- In case of LDCHK2, the loader is moved to the top of available memory (the top of stack 0, 1, 2, or 3 only) instead of the top of stack 0.

PARAMETERS

LODCHK2 has the same parameters as LODCHK.

ORGANIZATION

LODCHK2 has the same organization as LODCHK.

ACTION CODES

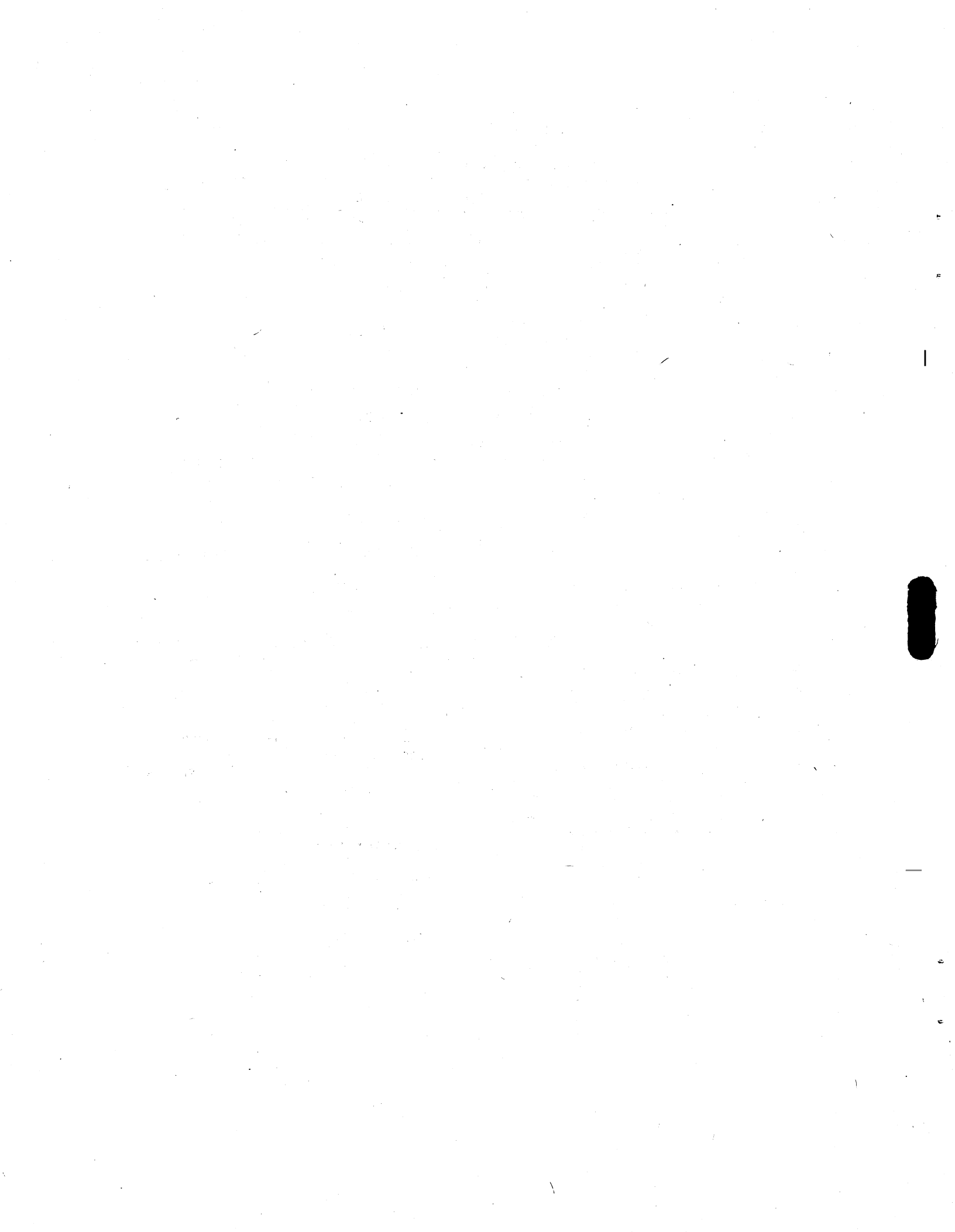
The action codes of LDCHK2 are those defined for LODCHK. The action codes in table 6-1 apply for LDCHK2 if the left-most digit of the action code (P value) is ignored.

ACTION MESSAGES

There are no action messages for LODCHK2.

RESTRICTIONS

LODCHK2 has the same restrictions as LODCHK.



Level I tests are loaded and executed sequentially. The order of execution of the tests may be random; however, the suggested order is:

1. MPINS
2. MPMEM
3. MPRTC

4. CRECO
5. LIAT2

The format of the output messages, error handling, section selection, run parameter definition, display, and modification are standard for all level I tests.

INSTRUCTION TEST

TEST IDENTIFICATION

01

TEST NAME

MPINS

PURPOSE

The instruction test validates the processor's macro instruction set (both basic and enhanced). See table 7-1 for a list of instructions and associated test sections.

PARAMETERS

MPINS uses one special parameter. It is a one-word flag used by the test to control the execution of the multi-level indirect addressing tests in sections 02 and 07. If the word is zero, then the multilevel indirect off tests are executed. If the word is one, the multi-level indirect on tests are executed. See table 7-2.

OVERLAYS

The overlay version contains the following overlays and test sections:

<u>Overlay No.</u>	<u>Test Section No.</u>
1	0 through 4
2	5 through 9

If more than one pass is specified for an overlay system, only those test sections in The message

MPINS SECTxxxxNOT FOUND

is issued for all tests in overlay 1 for each additional pass specified by the operator.

ORGANIZATION

The instruction test is broken up into nine sections organized as completely independent programs which should be run in order for the greatest effectiveness. There is an initialization section that is used to initialize the low core areas that are used by the test sections. The organization of instructions to be tested and their related test sections are shown in table 7-2.

Initialization Section

This section initializes the low core area to be used by the test sections. A table of a sliding one bit and a pointer to that table are placed into core starting at location 7. Figure 7-1 shows the core layout after execution of the initialization section.

Section 1 — Basic Register Reference and Inter-Register/Register Skips

Section 1 tests the operation of the basic register reference instructions and basic inter-register instructions. The instructions tested are shown in table 7-3.

TABLE 7-1. MPINS INSTRUCTION TEST ORGANIZATION

Mnemonic	Definition	Reference Test Section	OP Code			
AAB	Transfer Arithmetic Sum A, Q+M	1	0	8	3	8-F
AAM	Transfer Arithmetic Sum A, M	1	0	8	2	8-F
AAQ	Transfer Arithmetic Sum A, Q	1	0	8	3	0-7
ADD	ADD A	2	8	*		-Δ-
ADQ	ADD Q	2	F	*		-Δ-
ALS	A Left Shift	3	0	F	C/D	0-F
AMr	AND Memory	6	0	4	*	*
AND	AND with A	2	A	*		-Δ-
ANr	AND Register	6	0	4	*	*
ARr	Add Register	6	A	0		-Δ-
ARS	A Right Shift	3	0	4	*	*
ASC	Accumulator Scale	9	8	0		-Δ-
CAB	Transfer Complement Logical Product A, Q+M	1	0	F	4/5	0-F
CAM	Transfer Complement Logical Product A, M	1	0	B	0	A
CAQ	Transfer Complement Logical Product A, Q	1	0	8	F	8-F
CBP	Clear Breakpoint Interrupt	Not Tested	0	8	F	0-7
CCE	Compare Character Equal	6	0	B	0	7
CLF	Clear Field	7	0	4	*	*
CLR	Clear to Zero	1	E	2		-Δ-
CPB	Clear Program Protect	Protect Test	0	5	+	6
CrE	Compare Register Equal	6	#	#		-Δ-
DMI	Define Microinterrupt	Not Tested	0	8	4	0-7
DrP	Decrement and Repeat	4	0	7	0	0
DVI	Divide Integer	2	0	4	*	*
EAB	Transfer Exclusive OR A, Q, M	1	E	0		-Δ-
EAM	Transfer Exclusive OR A, M	1	0	B	0	6
					2, 4, 6, 8, A, C, E	S

TABLE 7-1. MPINS INSTRUCTION TEST ORGANIZATION (Continued)

Mnemonic	Definition	Reference Test Section	OP Code			
EAQ	Transfer Exclusive OR A, Q	1	0	8	7	0-7
EIN	Enable Interrupt	Not Tested	0	4	0	0
EMS	Execute Microsequence	9	0	B	r, o	2
ENA	Enter A	1	0	A		-Δ-
ENQ	Enter Q	1	0	C		-Δ-
EOR	Exclusive OR with A	2	B	*		-Δ-
EXI	Exit Interrupt State	Not Tested	0	E		-Δ-
GPE	Generate Character Parity Even	8	0	B	0	8
GPO	Generate Character Parity Odd	8	0	B	0	9
IIN	Inhibit Interrupt	Not Tested	0	5	0	0
INA	Increase A	1	0	9		-Δ-
INP	Input to A	Not Tested	0	2		-Δ-
INQ	Increase Q	1	0	D		-Δ-
JMP	Jump	1	1	*		-Δ-
LAB	Transfer Logical Product A, Q+M	1	0	8	B	8-F
LAM	Transfer Logical Product A, M	1	0	8	A	8-F
LAQ	Transfer Logical Product A, Q	1	0	8	B	0-7
LCA	Load Character to A	6	0	4	*	*
LDA	Load A	2	C	*		-Δ-
LDQ	Load Q	2	E	*		-Δ-
LFA	Load Field	7	0	5	*	4/0
LLB	Load Lower Unprotected Bounds	Protect Test	0	B	r, o	1
LLS	Long Left Shift	3	0	F	E/F	0-F
LMM	Load Micromemory	Not Tested	0	B	0	2
LRG	Load Register Group	5	0	B	0	2
LRr	Load Register	6	0	4	*	*
LRs	Load Right Shift	3	0	F	6/7	0-F
LUB	Load Upper Unprotected Bounds	Protect Test	0	B	r, o	0
MUI	Multiply Integer	2	2	*		-Δ-
NOP	No Operation	Not Tested	0	F	0/1	0-F

TABLE 7-1. MPINS INSTRUCTION TEST ORGANIZATION (Continued)

Mnemonic	Definition	Reference Test Section	OP Code			
OMr	OR Memory	6	0	4	*	*
			D	1	-Δ-	
ORr	OR Register	6	0	4	*	*
			D	0	-Δ-	
OUT	Output from A	Not Tested	0	3	-Δ-	
QLS	Q Left Shift	3	0	F	A/B	0-F
QRS	Q Right Shift	3	0	F	2/3	0-F
RAO	Replace Add 1 in Storage	2	D	*	-Δ-	
RTJ	Return Jump	2	5	*	-Δ-	
SAM	Skip if A = -	1	0	1	3	S
SAN	Skip if A ≠ +0	1	0	1	1	S
SAP	Skip if A = +	1	0	1	2	S
SAZ	Skip if A = +0	1	0	1	0	S
SBr	Subtract Register	6	0	4	*	*
			9	0	-Δ-	
SCA	Store Character from A	6	0	4	*	*
			C	3	-Δ-	
SEF	Set Field	7	0	5	*	7/F
			*	*	-Δ-	
SET	Set to 1s	1	0	8	8	0-7
SFA	Store Field	7	0	5	*	5/D
			*	*	-Δ-	
SFN	Skip if Field Not Zero	7	0	5	*	3/B
			*	*	-Δ-	
SFZ	Skip if Field Zero	7	0	5	*	2/A
			*	*	-Δ-	
SIO	Set/Sample Output or Input	Not Tested	0	B	0	4
SJE	Subroutine Jump Exit	6	0	4	*	*
			5	0	-Δ-	
SJr	Subroutine Jump	6	0	4	*	*
			5	0	-Δ-	
SLS	Select Stop	Not Tested	0	0	0	0
SNF	Skip on No Program Protect Fault	Protect Test	0	1	B	S
SNO	Skip on No Overflow	2	0	1	F	S
SNP	Skip on No Storage Parity Error	Memory Test	0	1	D	S
SOV	Skip on Overflow	8	0	1	A	S

TABLE 7-1. MPINS INSTRUCTION TEST ORGANIZATION (Continued)

Mnemonic	Definition	Reference Test Section	Op Code			
			7	*	-Δ-	
SPA	Store A, Parity to A	8	7	*	-Δ-	
SPB	Set Program Protect	Protect Test	0	6	0	0
SPE	Skip on Storage Parity Error	Memory Test	0	1	C	S
SPF	Skip on Program Protect Fault	Protect Test	0	1	E	S
SPS	Sample Position Status	Not Tested	0	B	0	5
SQM	Skip if Q = -	1	0	1	7	S
SQN	Skip if Q ≠ +0	1	0	1	5	S
SQP	Skip if Q = +	1	0	1	6	S
SQZ	Skip if Q = +0	1	0	1	4	S
SRG	Store Registers	5	0	B	0	3
SrM	Skip if Register Negative	4	0	0	3, 7, B, F	S
SrN	Skip if Register Nonzero	4	0	0	1, 5, 9, D	S
SrP	Skip if Register Positive	4	0	0	2, 6, A, E	S
SRr	Store Registers	5	}	0	4	* *
SrZ	Skip if Register Zero	4		C	1	-Δ-
STA	Store A	2	6	*	-Δ-	
STQ	Store Q	2	4	*	-Δ-	
SUB	Subtract	2	9	*	-Δ-	
SWN	Skip if Switch Not Set	LODCHK	0	1	9	S
SWS	Skip if Switch Set	LODCHK	0	1	8	S
TCA	Transfer Complement A	1	0	8	6	0-7
TCB	Transfer Complement Q+M	1	0	8	5	8-F
TCM	Transfer Complement M	1	0	8	4	8-F
TCQ	Transfer Complement Q	1	0	8	5	0-7
TRA	Transfer A	1	0	8	A	0-7
TRB	Transfer Q+M	1	0	8	9	8-F
TRM	Transfer M	1	0	8	8	8-F
TRQ	Transfer Q	1	0	8	9	0-7
XFr	Transfer Register	4	0	7	0, 1-7, 1-7	

TABLE 7-2. MPINS RUN PARAMETER LIST

Word	Initial Value (Hex)	Definition
TESTID	0001	Test ID
PASCNT	0000	Pass Count
ERRCNT	0000	Error Count
1	2080	Control Word
2	0001	Repeat Count
3	1234	Sections Selected
4	5678	Sections Selected
5	9000	Sections Selected
6	0000	Sections Selected
7	0000	Equipment Address
8	0000	Interrupt Lines (Micro/Macro)
9	0000	Logical Unit
A	FFFF	Include Multilevel Indirect Addressing Switch on Checks if Nonzero. Include Multilevel Indirect Addressing Switch off Checks if Zero

Section 1 is broken up into 18 parts and each part consists of a number of subsections. Each part tests a particular set of instructions together and each subsection is individually repeatable. The 18 parts are listed in table 7-4.

TABLE 7-3. BASIC REGISTER AND INTER-REGISTER INSTRUCTIONS

Register Reference	Inter-Register Reference
ENA	SET
ENQ	CLR
INA	TRr
INQ	TCr
	r = A, Q, M, or B
	AAr
	EAr
	LAr
	CAr
	r = Q, M, or B

ADDRESS (HEX)

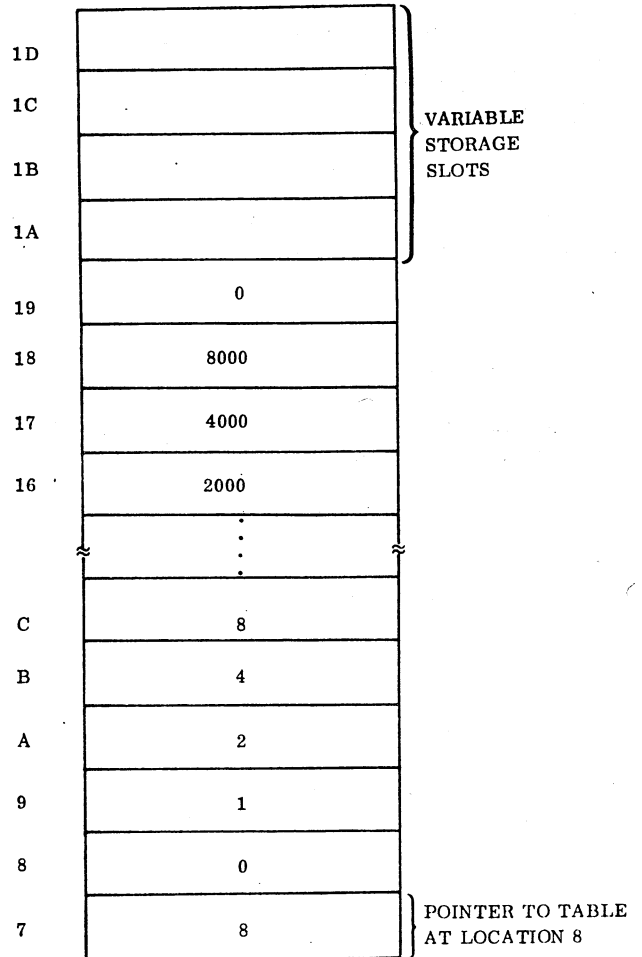


Figure 7-1. Core Layout After MPINS Initialization Section Execution

Section 2 — Basic Memory Reference Instructions and Addressing Mode

Section 2 tests the operation of the basic memory reference instructions and five addressing modes. The section is made up of 13 parts (the SPA instruction is tested in section 8 and the JMP instruction is tested in LDCHK and section 1). The addressing modes tested use all possible indexing schemes (I, Q, both, or no registers). Section 2 tests in the following order.

1. One-word absolute addressing
2. Two-word absolute addressing
3. Constant addressing
4. One-word relative addressing
5. Two-word relative addressing

Table 7-5 shows the order of testing and the correlation between instruction and addressing mode.

Section 3 — Shift Instructions

This section tests the operation of the basic A/Q register shift instructions which include:

- ARS — A right shift
- QRS — Q right shift
- LRS — Long right shift
- ALS — A left shift
- QLS — Q left shift
- LLS — Long left shift

Each instruction is tested with all shift counts (0 to 31) and 12 different data patterns. These patterns are:

- 0000₁₆
- FFFF₁₆
- 7FFF₁₆
- 8000₁₆
- 5555₁₆
- AAAA₁₆
- 3333₁₆
- CCCC₁₆
- 6666₁₆
- 9999₁₆
- 35AC₁₆
- CA53₁₆

The test of any shift instruction with one particular shift count and data pattern is repeatable as a subsection.

TABLE 7-4. BASIC REGISTER AND INTER-REGISTER TEST PARTS

Part	Instruction Tested	No. of Subsections
1	JMP* Test	1
2	ENA and A Register Skip Tests	4
3	ENQ and Q Register	4
4	ENA and SET A Tests	3
5	ENQ and SET Q Tests	2
6	ENA and CLR A Tests	2
7	ENQ and CLR Q Tests	2
8	ENA and INA Tests	3
9	ENQ and INQ Tests	3
10	ENA and SET/CLR/INA Tests	1
11	ENQ and SET/CLR/INQ Tests	1
12	Skip Counts Test	1
13	TRr Tests	20
14	TCr Tests	9
15	AAr Tests	3
16	EAr Tests	3
17	LAr Tests	3
18	CAr Tests	3

Section 4 — Decrement and Repeat and Basic Inter-Register and Skips

This section tests the operation of the decrement and repeat if positive instruction, the enhanced inter-register instruction, and the enhanced register skip instructions as listed below:

Enhanced Inter-Register	Decrement and Repeat if Positive	Enhanced Register Skip
XF1	D1P	S1Z S1P
XF2	D2P	S2Z S2P
XF4	D3P	S3Z S3P
XFQ	D4P	S4Z S4P
XFA	DQP	S1N S1M
XFI	DAP	S2N S2M
	DIP	S3N S3M
		S4N S4M

TABLE 7-5. BASIC MEMORY REFERENCE INSTRUCTION AND MODE

Instruction	No. of Subsections	Addressing Modes Used
Load A†	5	Short Absolute (All Indexes Used) Constant (No Index)
Store A	4	Short Relative (All Indexes Used)
Return Jump	1	Short Relative (No Index)
Exclusive Or A	5	Short Absolute Indirect (All Indexes Used)
And to A	5	Short Relative (All Indexes Used) Constant (I Indexing Used)
Load Q	5	Short Relative Indirect (All Indexes Used)
Store Q	4	Long Absolute (All Indexes Used)
Add to A	5	Short Absolute (Q and Q+I Indexing) Constant (Q Indexing)
Add to Q	1	Short Absolute Indirect (I Indexing Used) Constant (I Indexing Used)
Replace Add One	1	Long Absolute (No Index)
Subtract From A	5	Long Relative Indirect (All Indexes Used) Constant (No Index Used)
Multiply	2	Long Relative (I Indexing Used) Constant (B Indexing Used)
Divide	2	Long Relative Indirect (I Indexing Used) Constant (B Indexing Used)

†One-word absolute indirect for the special multi-level indirect tests

Section 4 is made up of four parts. Part 1 is a test of the XFA instruction with both the basic and enhanced registers being used as a destination. All of the registers are set to a background value and then one of them is set to the inverse value. This is done for four data values: $AAAA_{16}$, 5555_{16} , $FFFF_{16}$ and 0000. One register destination combined with one data value is repeatable at the subsection level.

Part 2 of the section tests the other XFR instructions (all source registers with all destination registers). For each combination of source and destination, the source and destination registers are set to $AAAA_{16}$ and the other registers are set to 5555_{16} . One combination of source and destination is repeatable as a subsection.

Part 3 tests the skip instructions for the enhanced registers. Each of the four enhanced registers is loaded with the same data patterns used in part 1 and all four skips are attempted on it. A combination of one register, one data pattern and one skip type is repeatable as a subsection.

Part 4 tests the DRP instructions. Each register is loaded with 2, 1, 8000_{16} , and 0000; and the corresponding decrement and repeat instruction is executed. The final value of the register and whether or not it is repeated is verified. A combination of one register and one data value is repeatable as a subsection.

Section 5 — Load and Store Register Group

Section 5 tests the operation of the load register group (LRG) and store register group (SRG) instructions. Each instruction is tested with overflow both set and cleared. The final values of the registers (LRG) or a core buffer (SRG) as well as the buffer pointer word are verified. Each combination of instruction and overflow values is repeatable as a subsection.

Section 6 — Enhanced Memory Reference Addressing and Instruction

Section 6 tests the operation of the enhanced memory reference instructions and their addressing modes. The correlation between instruction and mode is listed in table 7-6.

Section 7 — Enhanced Field Reference

Section 7 tests the operation of the enhanced field reference instructions and their addressing modes. The correlation between instruction and mode is given in table 7-7.

TABLE 7-6. ENHANCED MEMORY REFERENCE INSTRUCTION AND MODE

Instruction	Mode Used	Subsection No.
LRr	Short Absolute with All Indexes	1 through 56
SJr/SJE	Short Relative	57
ARr	Short Absolute Indirect	58
SBr	Short Relative Indirect	59
ANr	Constant Addressing	60
AMr	Long Absolute, Indexed	61
SRr	Long Relative	62
LCA	Long Relative Indirect	63 through 64
SCA	Short Absolute Indirect	65 through 66
ORr	Short Relative	67
OMr	Long Absolute	68
CrE	Long Relative, Indexed	69 through 70
CCE	Long Relative Indirect, Indexed	71 through 72

TABLE 7-7. ENHANCED FIELD REFERENCE INSTRUCTIONS

Instruction	Addressing Mode
SEF	Short Relative
CLF	Long Relative
SFZ	Short Absolute Indirect
SFN	Long Absolute
LFA	Long Relative
SFA	Long Relative Indirect

Section 8 — Parity Generation

Section 8 tests the operation of the parity generation instructions, which include SPA, GPE, and GPO. Each instruction is tested with each 4-bit part of the A register ranging from 0 through F and all other 4-bit parts equal to 0. A particular instruction together with one of the 64 data values can be repeated as a subsection.

Section 9 — Miscellaneous Instructions

Section 9 is composed of two parts. The first part tests the operation of the execute micro sequence (EMS) instruction. The EMS instruction is executed twice, going to two different places in the emulator. Either one of the places may be repeated as a subsection.

The second part of section 9 tests the A scale instruction. The A register is scaled once with A equal to -0 (FFFF₁₆) and once with A equal to 1. Either data value is repeatable as a subsection.

MESSAGES

Action Codes

The action codes for MPINS are listed in table 7-8. All action codes generated by the instruction tests are of the following form:

nnxy

TABLE 7-8. MPINS OUTPUT MESSAGES

Action Code	Test Section	English Text	Description	Additional Information
01x1	1	ENA	ENA failure	EXPA = Expected value of A register ACTA = Actual value of A register EXPQ = Expected value of Q register ACTQ = Actual value of Q register EXPM = Expected value of M register ACTM = Actual value of M register
		ENQ	ENQ failure	
01x2	1	ALL SKIPS	All skip counts failed.	
		SKIP(S)	Some skips failed.	
01x3	1	JMP	JMP* failure	
		SET	SET A or SET Q failure	
		CLR	CLR A or CLR Q failure	
		INA	INA failure	
		INQ	INQ failure	
		TRA	TRA failure	
		TRQ	TRQ failure	
		TCA	TCA failure	
		TCQ	TCQ failure	
		AAQ	AAQ failure	
		EAQ	EAQ failure	
		EAB	EAB failure	
		LAQ	LAQ failure	
		CAQ	CAQ failure	
		01x3	2	
STA	STA failure			
LDQ	LDQ failure			
STQ	STQ failure			
RAO	RAO failure			
EOR	EOR failure			
AND	AND failure			
ADD	ADD failure			
ADQ	ADQ failure			
SUB	SUB failure			
OV ON = xxx } OV OFF = xxx }	Overflow error using instruction xxx			
MUI	Multiply failure			
				EXPV = Expected value ACTV = Actual value OP1 = Operand 1 OP2 = Operand 2 originally in memory OP1A = Operand originally in A

TABLE 7-8. MPINS OUTPUT MESSAGES (Continued)

Action Code	Test Section	English Text	Description	Additional Information
01x3		RTJ	Return Jump failure	
		OVBAD	Overflow status error	
01x3	4	XFR r	Inter-register instruction failure r = 1, 2, 3, 4, Q, A, or I	EXP1 = Expected value of register 1 ACT1 = Actual value of register 1 EXP2 = Expected value of register 2 ACT2 = Actual value of register 2 EXP3 = Expected value of register 3 ACT3 = Actual value of register 3 EXP4 = Expected value of register 4 ACT4 = Actual value of register 4 EXPQ = Expected value of Q ACTQ = Actual value of Q EXPA = Expected value of A ACTA = Actual value of A EXPI = Expected value of I ACTI = Actual value of I
		DRP	Decrement and repeat instruction failure r = 1, 2, 3, 4, Q, A, or I	
		SRX	Skip instruction failure r = 1, 2, 3, 4, Q, A, or I x = x, N, M, or P	VALU = Value in register R
		DRP REPEATED	DRP failure	
		DRP NO RPT	r = 1, 2, 3, 4, Q, A, or I	
		I REG ERROR-XXX	I register failure during the testing of instruction xxx.	I REG = Value of location FF FILE = Value in file 2
01x3	5	LRGP	LRG pointer error	EXPP = Expected pointer value
		SRGP	SRG pointer error	ACTP = Actual pointer value
		LRGR	LRG register error	xxxx = Null word
		SRGR	SRG register error	EXP1 = Expected value of register 1 EXP2 = Expected value of register 2 EXP3 = Expected value of register 3 EXP4 = Expected value of register 4 EXPQ = Expected value of Q EXPA = Expected value of A EXPI = Expected value of I EXPM = Expected value of M EXPO = Expected overflow flag YYYY = Null word ACT1 = Actual value of register 1 ACT2 = Actual value of register 2 ACT3 = Actual value of register 3 ACT4 = Actual value of register 4

TABLE 7-8. MPINS OUTPUT MESSAGES (Continued)

Action Code	Test Section	English Text	Description	Additional Information
01x3				ACTQ = Actual value of Q ACTA = Actual value of A ACTI = Actual value of I ACTM = Actual value of M ACTO = Actual overflow flag
01x3	6	LRr	Load Register r failure r = 1, 2, 3, 4, Q, A, or I	PREG = Register number of destination register XREG = Register number of index register
		SJA NO JUMP	SJA instruction failed to jump	CREG = Register number of character index
		SJA	SJA failure	= Null Word
		AR1	AR1 failure	= Null Word
		SB2	SB2 failure	= Null Word
		AN3	AN3 failure	EXP1 = Expected value of register 1
		AM4	AM4 failure	ACT1 = Actual value of register 1
		SRA	SRA failure	EXP2 = Expected value of register 2
		LCA	LCA failure	ACT2 = Actual value of register 2
		SCA	SCA failure	EXP3 = Expected value of register 3
		ORQ	ORQ failure	ACT3 = Actual value of register 3
		OMI	OMI failure	EXP4 = Expected value of register 4
		C3E NO COMPARE	C3E failed to compare	ACT4 = Actual value of register 4
		C3E	C3E failure	EXPQ = Expected value of Q
		CCE NO COMPARE	CCE failed to compare	ACTQ = Actual value of Q
		CCE	CCE failure	EXPA = Expected value of A
				ACTA = Actual value of A
				EXPI = Expected value of I
				ACTI = Actual value of I
				EXPM = Expected value of M
				ACTM = Actual value of M
				EMEM = Expected value of memory
				AMEM = Actual value of memory
01x3	7	SEF	SEF failure	EXPT = Expected value
		CLF	CLF failure	ACTL = Actual value
		SFZ	SFZ failure	
		SFN	SFN failure	
		LFA	LFA failure	
		SFA	SFA failure	
01x3	8	SPA PARITY ERROR	Incorrect parity using SPA instruction	DATA = Data used to generate the parity

TABLE 7-8. MPINS OUTPUT MESSAGES (Continued)

Action Code	Test Section	English Text	Description	Additional Information
01x3		GPE PARITY ERROR	Incorrect parity using GPE instruction	
		GPO PARITY ERROR	Incorrect parity using GPO instruction	
		SPA STORE ERROR	Data store by SPA instruction incorrect	EXPV = Expected value in memory ACTV = Actual value in memory
01x3	9	EMS	Execute micro sequence error	EXP1 = Expected value of register 1 ACT1 = Actual value of register 1 EXP2 = Expected value of register 2 ACT2 = Actual value of register 2 EXP3 = Expected value of register 3 ACT3 = Actual value of register 3 EXP4 = Expected value of register 4 ACT4 = Actual value of register 4 EXPQ = Expected value of Q ACTQ = Actual value of Q EXPA = Expected value of A ACTA = Actual value of A EXPI = Expected value of I ACTI = Actual value of I EXPM = Expected value of M ACTM = Actual value of M
		ASC	A scale error	
01x4	1	TRM	TRM failure	Same as error code
		TRB	TRB failure	01x3 for section 1 with an English text of TRA
		TCM	TCM failure	
		TCB	TCB failure	
		AAM	AAM failure	
		AAB	AAB failure	
		EAM	EAM failure	
		EAB	EAB failure	
		EAM	EAM failure	
		LAM	LAM failure	
		LAB	LAB failure	
		CAM	CAM failure	
		CAB	CAB failure	
01x4	2	MLI	Multi-level indirect test error	EXPV = Expected value ACTV = Actual value Same as error 01x3, section 2 for MUI.
		DVI	Divide failure	OP1Q = Operand originally in Q

TABLE 7-8. MPINS OUTPUT MESSAGES (Continued)

Action Code	Test Section	English Text	Description	Additional Information
01x4	3	NOS	A shift instruction specifying no shift failed	BEGQ = Beginning value of Q EXPQ = Expected result in Q ACTQ = Actual result in Q BEGA = Beginning value of A EXPA = Expected result in A ACTA = Actual result in A SC = Shift count
		QRS	QRS failure	
		ARS	ARS failure	
		LRS	LRS failure	
		QLS	QLS failure	
		ALS	ALS failure	
		LLS	LLS failure	

Where: nny is the test identification

x is the failure mode flag

1 = The error occurred on either the first test of an instruction or all tests of it.

2 = The error occurred on a test other than the first or did not fail all of the tests.

y is the error code.

The instruction test uses an area of low core from location 7 to location $1D_{16}$ regardless of where it is loaded in core, thereby destroying any data or code that resides there.

If more than one pass of a test is specified in an overlay version, only those test sections in overlay 2 are included. A message of

MPINS SECTxxxx NOT FOUND

is issued for all sections in overlay 1.

RESTRICTIONS

The instruction test must be loaded starting at the first word of a stack, but should not be loaded at an address greater than $5FFF_{16}$.

MAIN MEMORY TEST

TEST IDENTIFICATION

05

TEST NAME

MPMEM

PURPOSE

MPMEM verifies that every specified word (run parameters A and B) of macro memory and the addressing lines are functioning properly. MPMEM stores, loads, and compares various bit patterns that are defined by the particular sections selected to be executed. After a load or store operation has been performed to one location, MPMEM checks to see if a parity error has occurred.

PARAMETERS

The run parameters list is illustrated in table 7-9.

Run parameters A, B, and E of the parameter list are used for verification before test execution can be started. Words A and B are checked in the following manner:

Start Address Stop Address
 Word A ≤ Word B ≤ Address
 of last location in memory

If any of the conditions are not true, an action message is issued and the operator must re-enter parameter list entries A and B.

The computed number of stacks of memory in the machine is checked against run parameter E in the parameter list. If they do not match, MPMEM is suspended, an action code is issued giving the expected value for parameter E, the run parameters are displayed, and the operator must re-enter run parameter E of the parameter list.

TABLE 7-9. MPMEM RUN PARAMETER LIST

Word	Initial Value (Hex)	Description
TESTID	0005	Test ID
PASCNT	0000	Pass Count
ERRCNT	0000	Error Count
1	2080	Control Word
2	0001	Repeat count
3	1234	Sections Selected
4	5000	Sections Selected
5	0000	Sections Selected
6	0000	Sections Selected
7	0000	Equipment Address
8	0000	Interrupt Lines (Micro/Macro)
9	0000	Logical Unit
A	0000	Start Address — First Word of Main Memory to be Tested
B	1FFF	Stop Address — Last Word of Main Memory to be Tested†
C	5555	Special Test Pattern 1 — First Word of Special Pattern Test
D	BBBB	Special Test Pattern 2 — Second Word of Special Pattern Test
E	0001	Number of Stacks in Memory††

†From the starting address (word A) up to and including the ending address (word B) is tested.
 ††Stack refers to 8K of memory.

OVERLAYS

The overlay version contains the following overlays and test sections.

Overlay No.	Test Section No.
1	0
2	1
3	2
4	3
5	4
6	5, 10

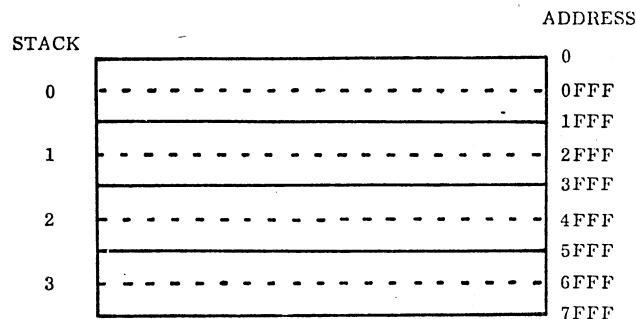


Figure 7-2. 32K Core Map Description

ORGANIZATION

MPMEM consists of five test sections.

In order to test all of memory specified by the operator, MPMEM may be required to move itself, the loader, and the parameter lists to some locations other than the one in which they were loaded. Thus, the operator cannot arbitrarily master clear and restart the test while it is executing a section. However, MPMEM can be restarted when it comes to a normal stop; i. e., upon completion of a section or the test. The test cannot be restarted from an error stop but continues from the error stop location +1.

The common control directs the flow of the test. Upon completion of the test, the loader and the parameter lists are moved back to the top of the stack, and the test is moved back to the lower half of the stack. MPMEM calls the loader to load the next diagnostic, if any.

NOTE

Stack refers to the 8K memory stack into which the test was originally loaded.

Section 1 — Addressing

In order to protect the memory test program from being altered because of an addressing problem, special precaution has to be taken in conducting the addressing test. The following shows how addressing problems are diagnosed (CDC 1700 bit numbering is used in the following discussion).

Assuming that there are 32K in the machine, figure 7-2 shows the core map before the addressing test section

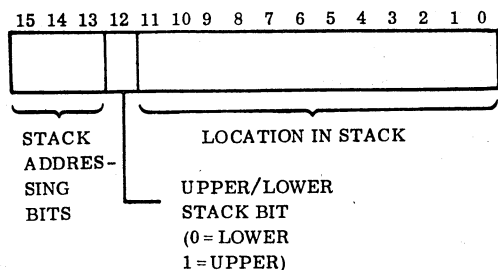
is executed. Figure 7-3 shows the bit configuration of an address in relationship to a stack.

Stack test addressing performs the following functions regardless of the start and stop addresses:

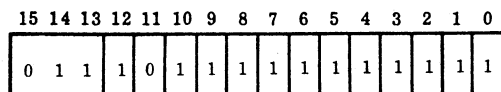
1. Writes $7FFF_{16}$ in location $7FFF_{16}$
2. Reads location $7FFF_{16}$ and verifies that it is $7FFF_{16}$. If correct, proceed with step 3. If wrong, note error (may be addressing line or memory) and continue at step 3.
3. Reads locations $5FFF_{16}$, $3FFF_{16}$, $1FFF_{16}$, and compares with their contents stored in the program
4. If there is no error, steps 1, 2, and 3 are repeated three times, replacing location $7FFF_{16}$ with locations $5FFF_{16}$, $3FFF_{16}$, and $1FFF_{16}$, respectively.
5. If any of the two values do not match, an addressing line error occurs.

Interstack addressing validation proceeds as follows:

1. Set $n = \text{START address}$ specified by the operator.
2. Write n in location n .
3. Increment n by one.
4. Go to step 2 until n is greater than the STOP address specified by the operator.
5. Read all locations in the test area and verify that the contents are correct.
6. Set $n = \text{STOP address}$.
7. Write n in location n .



FOR EXAMPLE, IF THE STACK ADDRESS WORD WERE



IT WOULD INDICATE:
STACK 3
UPPER HALF OF STACK
ADDRESS 07FF

Figure 7-3. Stack Addressing Bits

8. Decrement n by one.
9. Go to step 7 until n is less than the START address.
10. Read all locations in the test area and verify that the contents are correct.
11. Output an error if any failure.

Section 2 — Worst Case Test

Section 2 stores $FFFF_{16}$ or 0000_{16} in all words of the test area, and retrieves and verifies the results. The complement pattern is also stored, retrieved, and verified.

The Core Memory Specification defines the worst case test pattern. If bits 6 and 10 of the effective address of the word to be tested were equal (either 1, 1 or 0, 0), then the worst case test pattern would be $FFFF_{16}$. If

they were unequal, (either 1, 0 or 0, 1), then the pattern would be 0000_{16} .

Section 3 — Constant Pattern Alteration

Two constant patterns specified via the parameter list are used to test core. The first test pattern is stored, retrieved, and verified for all locations in the test area; then the second test pattern is tested.

Section 4 — Roll Test

Section 4 changes the bit status as quickly as possible by storing, retrieving, and comparing the following 34 patterns in the order presented:

1. 7FFF
2. 8000
3. BFFF
4. 4000
- ⋮
31. FFFE
32. 0001
33. FFFF
34. 0000

Memory is tested one word at a time using all 34 patterns.

Section 5 — Alternate AAAA and 5555 Test

Section 5 first writes AAAA in the first location of the test area, 5555 in the second, AAAA in the third, etc., until the test area has been completely filled. The patterns are then read and verified to make sure that the test area contents are in the alternating pattern. The test area is then rewritten and verified using 5555 and AAAA.

MESSAGES

Action Codes

Table 7-10 shows the MPMEM action codes.

RESTRICTIONS

MPMEM restrictions are as follows:

1. The operator cannot master clear and restart the test from location 0 while MPMEM is executing a section or restarted (from location 0) after an error stop (however, MPMEM can be restarted when it comes to a normal stop; i. e., upon completion of a section or the test).
2. The last location in each stack is altered.
3. The contents of last locations of all stacks are altered.
4. When testing more than 32K of memory, suppress multilevel indirect addressing before starting the test.

TABLE 7-10. MPMEM OUTPUT MESSAGES

Action Code	Test Section	English Text	Description	Additional Information
0540	2-5	BAD DATA	Error in stack 0 (locations 0000 ₁₆ through 1FFF ₁₆)	ADDR = Location of bad data EXVA = Expected value of data ACVA = Actual value of data
0541	2-5	BAD DATA	Error in stack 1 (locations 2000 ₁₆ through 3FFF ₁₆)	
0542	2-5	BAD DATA	Error in stack 2 (locations 4000 ₁₆ through 5FFF ₁₆)	
0543	2-5	BAD DATA	Error in stack 3 (locations 6000 ₁₆ through 7FFF ₁₆)	
0544	2-5	BAD DATA	Error in stack 4 (locations 8000 ₁₆ through 9FFF ₁₆)	
0545	2-5	BAD DATA	Error in stack 5 (locations A000 ₁₆ through BFFF ₁₆)	
0546	2-5	BAD DATA	Error in stack 6 (locations C000 ₁₆ through DFFF ₁₆)	
0547	2-5	BAD DATA	Error in stack 7 (locations E000 ₁₆ through FFFF ₁₆)	ADDR = Locations that caused parity error
0570	1-5	PARITY ERR	Parity error in stack 0	
0571	1-5	PARITY ERR	Parity error in stack 1	
0572	1-5	PARITY ERR	Parity error in stack 2	
0573	1-5	PARITY ERR	Parity error in stack 3	
0574	1-5	PARITY ERR	Parity error in stack 4	
0575	1-5	PARITY ERR	Parity error in stack 5	
0576	1-5	PARITY ERR	Parity error in stack 6	
0577	1-5	PARITY ERR	Parity error in stack 7	
0578	1-5	PARITY ERR	Parity error in undetermined location	
05A0	1	ADRING ERR	Addressing error in stack 0	ADDR = Address in error

TABLE 7-10. MPMEM OUTPUT MESSAGES (Continued)

Action Code	Test Section	English Text	Description	Additional Information
05A1	1	ADRING ERR	Addressing error in stack 1	EXVA = Expected address
05A2	1	ADRING ERR	Addressing error in stack 2	ACVA = Actual address
05A3	1	ADRING ERR	Addressing error in stack 3	
05A4	1	ADRING ERR	Addressing error in stack 4	
05A5	1	ADRING ERR	Addressing error in stack 5	
05A6	1	ADRING ERR	Addressing error in stack 6	
05A7	1	ADRING ERR	Addressing error in stack 7	
05E8		PARAM ERR	Total number of stacks specified by user if different from value computed by the program	EXVA = Number of stacks from parameter list ACVA = Number of stacks computed by the program.
05E9		PARAM ERR	Start and/or stop address specified by the user is wrong.	Irrelevant.

PROTECT TEST

TEST IDENTIFICATION

06

TEST NAME

MPRTC

PURPOSE

MPRTC tests the program protect system along with the interrupt system and real-time clock of the processor. The protect system is tested by:

1. Ensuring that setting or clearing the protect bit of a memory location does not alter the contents of that location
2. Attempting to execute the privileged instructions from unprotected locations
3. Attempting to execute a protected instruction following the execution of an unprotected instruction
4. Attempting to store into a protected location with an unprotected instruction
5. Validating that with the interrupt system disabled, a protect fault causes the instruction causing the fault to be treated as a selective stop. Validate that the clock generates interrupts and that no protect fault is generated if a program return (from unprotected memory to protected memory) is caused by the clock (macro level) interrupt.

For 2, 3, and 4 above, memory is left unprotected by the following two different methods:

1. By using the clear protect bit (CPB) instruction
2. By loading the lower and upper bound registers (to override the protect bit)

PARAMETERS

The special parameter for this test is run parameter A. A holds the ending address for the core area to be tested. Initial values for the parameters are illustrated in table 7-11.

OVERLAYS

No overlays are needed for the overlay version.

ORGANIZATION

The test is composed of a control section, an initializing section, a terminating section, and five test sections. The control section, which is the same for all level I tests, is responsible for run parameter display and entry, selection of test sections, control of number of test passes, and repetition of sections. Test sections are executed in the same order they are selected and the same section may be repeated if desired. The whole test may also be repeated.

Initialization Section

This is not a selectable section, but it is executed once before executing the test. It performs the following steps:

1. Moves the parameter lists and loader next to the test.
2. Asks the operator to clear the PROTECT switch and the STOP switch by issuing the following message:

```
CLEAR PROTECT AND STOP  
SWITCHES (ESC J20@ GO CR)
```
3. Suspend test waiting for the operator to perform the task (step 2).
4. Protect all available memory locations.

TABLE 7-11. MPRTC RUN PARAMETER LIST

Word	Initial Value (Hex)	Definition
TESTID	0006	Test ID
PASCNT	0000	Pass Count
ERRCNT	0000	Error Count
1	2080	Control Word
2	0001	Repeat Count
3	1234	Sections Selected
4	5000	Sections Selected
5	0000	Sections Selected
6	0000	Sections Selected
7	00F3	Equipment Address of Clock
8	0088	Interrupt Lines of Clock (Micro/Macro)
9	0000	Logical Unit
A	0000	Stop Address†

†The start address is set to the address of the last cell occupied by the test + 1. The stop address is automatically calculated by the computer when the default value (0000) is used; otherwise the address given is used as the stop address.

5. Make sure that setting the protect bit does not cause a parity error or change the contents of the memory location.
6. Start the clock.
7. Ask the operator to set the PROTECT switch and clear the SELECTIVE STOP switch by issuing the following message:

SET PROTECT AND CLEAR STOP SWITCHES (ESC J28@ GO CR)
8. Suspend test waiting for the operator to perform the task (step 7).
9. Enable interrupts.

Section 1 — A Set and Clear Bit Without Altering Cell Contents

This section makes sure that setting and clearing the protect bit of a memory cell does not alter the contents of that cell. It performs the following steps:

1. Set test pattern to 0000₁₆.
2. Store test pattern in a cell of the memory area delimited by the address of the last word of the test and the stop address specified in the parameter list.
3. Clear the protect bit in that cell.
4. Report any parity error.
5. Report any protect fault.
6. Report the error if the contents of the cell has changed.
7. Set the protect bit of the same cell.
8. Repeat steps 4 through 5.
9. Repeat steps 2 through 8 for all cells in test area.
10. Set the test pattern to FFFF₁₆.
11. Repeat steps 2 through 9.

Section 2 — Protect Fault Test of Privileged Instruction from Unprotected Location

This section tests the protect fault caused by the attempt to execute a privileged instruction from an unprotected location. These instructions are: EIN, IIN, SPB, CPB, EXI, LMM, LRG, SRG, SIO, SPS, DMI, CBP, GPE, GPO, LUB, LLB, EMS and all inter-register instructions that have the mask register (M) as a destination register.

The following steps are performed in this section:

1. Unprotect one memory location by loading the upper and lower bound registers.
2. Store one of the privileged instructions listed above in the unprotected location.
3. Attempt to execute this unprotected privileged instruction.

4. Expect an interrupt on line 0. An error is assumed if there is no interrupt.
5. Determine the cause of interrupt. It is an error if it is not a protect fault (parity error or undetermined).
6. Check the contents of location 100_{16} (line zero interrupt trap) against the expected value. Report an error if unequal.
7. Repeat steps 2 through 6 for the next privileged instruction until all instructions in the list are checked.
8. Make bound registers ineffective.
9. Clear the protect bit for the location from which the privileged instruction is executed.
10. Repeat steps 2 through 7.
11. Set the protect bit of the memory location.

Section 3 — Protect Fault Interrupt Caused by Protected Instructions

This section determines whether or not an attempt to execute a protected instruction following the execution of a nonprotected one causes a protect fault interrupt. The unprotected instruction is stored in the memory area delimited by the start and stop address specified in the parameter list. The following steps are performed in this section:

1. Unprotect one memory location (starting at the start address) by loading the upper and lower bound registers.
2. Store a jump instruction in that unprotected location. The jump is to a protected location.
3. Transfer control to the jump instruction.
4. Expect an interrupt on line 0. Assume an error if no interrupt occurs.
5. Determine the cause of interrupt. Assume an error if it is not a protect fault.
6. Check the contents of location 100_{16} against the expected value. Report an error if they are not equal.
7. Repeat steps 2 through 6 for the next available memory location until the stop address is reached.

8. Make the bound registers ineffective.
9. Repeat steps 2 through 7 but use the CPB instruction to unprotect the memory location.

Section 4 — Store in Protected Memory Protect Fault Interrupt

This section determines whether to store in protected memory (delimited by the start and stop addresses in the parameter list) by the execution of instructions in unprotected memory causes a protect fault interrupt. It also verifies that the contents of the memory location referenced by the instructions do not get altered. All the instructions that can alter a memory location are executed from an unprotected location. These are: RAO, SPA, STQ, STA, RTJ, and the following instructions of the enhanced set: The store register (SRr), and to memory (AMr), or to memory (OMr), store character (SCA), store field (SFA), clear field (CLR), and set field (SEF) instructions.

The following steps are performed in this section:

1. Unprotect one memory location by loading the bound registers.
2. Store one of the instructions listed above in this unprotected location and the next location (two words).
3. Attempt to execute that instruction.
4. Expect an interrupt on line 0. Assume and report an error if no interrupt occurs.
5. Determine the cause of interrupt. Assume an error if the cause is not a protect fault.
6. Compare the contents of location 100_{16} against the expected value. Report an error if they are unequal.
7. Verify that the contents of the memory location referenced by the instructions do not get altered.
8. Repeat steps 3 through 7 so that the effective address for the instruction is incremented throughout that area of memory specified by the parameter list for the STA instruction only.
9. Repeat steps 2 through 8 for the next instruction in the list until the whole list is exhausted.

10. Protect the unprotected location by loading the lower bound register with FFFF₁₆.
11. Clear the protect bit of the same location by using the CPB instruction.
12. Repeat steps 2 through 8 for all instructions in table.

Section 5 — Selective Stop Protect Fault and Jump

The task of this section is to validate the following two properties of the protect system:

1. An instruction causing a protect fault is treated as a selective stop by the processor if interrupts are disabled and the PROTECT switch is on.
2. If a program jump from unprotected memory to protected memory is caused by an interrupt, then no protect fault is generated.

To test the first feature, the program performs the following steps:

1. Issues the following message to the operator:

```
SET PROTECT AND STOP SWITCHES
(ESC J2A@ GO CR)
```

and suspends the test.

2. At this point, the operator must set the PROTECT and STOP switches and resume the test by entering:

```
ESCAPE
```

```
J2A@
```

```
GO (cr)
```

3. Disables interrupts.
4. Issues the following message to the operator:

```
VERIFY CPU HALTED AT xxxx (ESC
J11: K:) AND RESTART CPU (I@)
```

Where: xxxx is the address of the instruction that caused the protect fault.

5. Causes a protect fault by executing a privileged instruction from an unprotected memory location.

6. At this point the operator must inspect the P register by entering

```
ESCAPE
```

```
J11:
```

```
K:
```

Compare with the value displayed with that given in the message in step 4; then resume the test by entering

```
I@
```

7. Issues the following message to the operator:

```
SET PROTECT AND CLEAR STOP
SWITCHES (ESC J28@ GO CR)
```

To test the second feature, the test performs the following steps:

1. Starts the clock.
2. Enable interrupts.
3. Unprotects an area in memory that contains a waiting loop.
4. Goes into the waiting loop.
5. The clock now interrupts. Control is transferred to the interrupt handler in protected memory. No protect fault should occur. An error is reported if a protect fault occurs or the clock does not interrupt.

Terminating Section

This is not a selectable section; it is designed to undo what the initialization section does. It is normally executed just before the test is terminated and performs the following steps:

1. Stops the clock.
 2. Disables interrupts.
 3. Moves the parameter lists and loader back to the top of the stack.
 4. Issues the following message to the operator:
- ```
CLEAR PROTECT AND SET STOP
SWITCHES (ESC J22@ GO CR)
```
5. Suspends test waiting for the operator to perform the task of the previous step.

## MESSAGES

The test does not operate properly if loaded in a memory stack other than stack 0.

## Action Codes

The test cannot use 7FFF or FFFF as a stop address due to upper bound register restrictions.

Table 7-12 lists all the action codes generated by the protect test.

## RESTRICTIONS

The test is a stand-alone test; it does not run under a controlling monitor, nor does it run with other tests.

TABLE 7-12. MPRTC OUTPUT MESSAGES

| Action Code | English Text      | Description                                                                                                                                                           | Additional Information                                                                          |
|-------------|-------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------|
| 0621        | CLOCK REJECT      | External or internal reject from the clock                                                                                                                            | None                                                                                            |
| 0641        | CPB CHNGD MEMORY  | The clear protect bit instruction has modified memory. The actual and expected contents of memory and the memory location are displayed.                              | ACTL = Actual value of memory<br>EXPD = Expected value of memory<br>ADDR = Address being tested |
| 0642        | SPB CHNGD MEMORY  | The set protect bit instruction has modified memory. The actual and expected contents of memory and the memory location are displayed.                                | Same as for code 0641                                                                           |
| 0651        | NO PROTCT FLT-CPB | An expected protect fault did not occur. The method of unprotected memory was via a CPB instruction.                                                                  | INST = Instruction that failed to cause a fault.                                                |
| 0652        | NO PRTCT FLT-BND  | An expected protect fault did not occur. The method of unprotected memory was bound registers.                                                                        | INST = Instruction that failed to cause a fault                                                 |
| 0653        | BAD LOC \$0100    | An expected protect fault occurred but the return address in location 100 <sub>16</sub> is not the expected address. The actual and expected addresses are displayed. | ACTL = Actual value of location 100<br>EXPD = Expected value of location 100                    |
| 0654        | PROTECT FAULTS    | Unexpected interrupts occurred because of illegal protect faults.                                                                                                     | CNTR = Number of protect faults<br>\$100 = Contents of location 100                             |
| 0655        | POWER FAILURE     | Power failure interrupts have occurred. (No protect fault or parity error detected after an interrupt.)                                                               | CNTR = Number of power failures<br>\$100 = Contents of location 100                             |

TABLE 7-12. MPRTC OUTPUT MESSAGES (Continued)

| Action Code | English Text     | Description                                                                                                                                                                                                    | Additional Information                                              |
|-------------|------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------|
| 0656        | STORE EXECUTED   | An instruction modifying protected memory got executed from an unprotected location. The instruction and the contents of the memory location before and after the execution of store instruction are displayed | INST = Instruction that modified memory                             |
| 0657        | NO CLOCK INTRPT  | The clock is not providing a macro level interrupt. The interrupt is expected once each 3.3 milliseconds and this error is output if the interrupt does not occur within 10 milliseconds.                      | None                                                                |
| 0661        | INCOMP. SNF/SPF  | There is a conflict between the usage of the skip on no protect fault (SNF) and the skip on protect fault (SPF) instructions being used to determine a protect fault.                                          | None                                                                |
| 0671        | PARITY ERROR     | A memory parity error has occurred.                                                                                                                                                                            | CNTR = Number of parity errors<br>\$100 = Contents of location 100  |
| 0672        | PARITY ERRORS    | A number of parity error interrupts has occurred.                                                                                                                                                              | CNTR = Number of parity errors<br>\$100 = Contents of location 100. |
| 06A1        | BAD STOP ADDR    | A stop address greater than the maximum available core or less than the address of the last word of the program has been specified in word A of the run parameter list.                                        | MINI = Minimum value allowed<br>MAXI = Maximum value allowed        |
| 06B1        | CONS INT, POWER  | Constant interrupt on line 0; power failure indicated                                                                                                                                                          | None                                                                |
| 06B2        | CONS INT, PROTEC | Constant interrupt on line 0; protect fault is indicated                                                                                                                                                       | None                                                                |
| 06B3        | CONS INT, PARITY | Constant interrupt on line 0; parity error is indicated                                                                                                                                                        | None                                                                |

## CDT TEST

### TEST IDENTIFICATION

07

### TEST NAME

LIAT2

### PURPOSE

LIAT2 is an ODS stand-alone, level I program. It is designed to test the I/O controller of the processor and the subassemblies of the LIAT Display Model II/Keyboard Model III.†

The BATCH MODE switch is activated during the test. The terminal is thus maintained in character mode and full duplex with the scroll feature disabled. The PARITY ENABLE/DISABLE switch is set to ENABLE and the PARITY EVEN/ODD switch is set to EVEN.

The program tests the I/O controller by issuing director functions and verifying that all appropriate functions have been performed. The subassemblies are tested by displaying predefined patterns on the screen, and the operator is to judge whether the subassemblies have performed satisfactorily. The keyboard is tested by having the operator input some messages and the program verifying that it is correct.

### PARAMETERS

Table 7-13 illustrates the LIAT run parameter list.

Repeat count, control flags, and sections selected are in the format for level I tests.

---

†The LIAT self test as described in the hardware maintenance manual should be run prior to LIAT2 execution.

## OVERLAYS

No overlays are needed for the overlay version.

## ORGANIZATION

There are nine sections in this test. The control section, which is common to all level I tests, directs the flow of the test.

### Section 1 — Controller Command/Status Test

This section verifies that the controller recognizes director functions and performs them correctly. The following director functions are issued one at a time: clear controller, clear interrupt, select read mode, and select write mode. After each director function has been issued, the director status is read. The program checks that the controller has performed all the functions related to that director function. If the appropriate functions were not performed, then the error would be reported.

### Section 2 — Terminal Display Command Test

There are five subsections in this test. The subsections test the following functions: bell, skip, backspace, line clear, screen clear, cursor return, and cursor reset. There is sufficient waiting time between the operations so that the operator can view the terminal operations. After one subsection has been executed, the program waits *n* seconds (where *n* is parameter B) for the operator to judge whether the terminal operation is successful or not.

If the terminal failed the timing criteria set by the operator, then the operator should follow the instructions in the hardware maintenance manual.

The subsections are executed in the following order:

#### Bell

The bell rings 80 times continuously. The operator should judge the tone and loudness of the sonic tone. The long bell tone is repeated three times.

TABLE 7-13. LIAT RUN PARAMETER LIST

| Word   | Initial Value (Hex) | Definition                           |
|--------|---------------------|--------------------------------------|
| TESTID | 0007                | Test ID                              |
| PASCNT | 0000                | Pass Count                           |
| ERRCNT | 0000                | Error Count                          |
| 1      | 2082                | Control Word                         |
| 2      | 0001                | Repeat Count                         |
| 3      | 1234                | Sections Selected                    |
| 4      | 5678                | Sections Selected                    |
| 5      | 9000                | Sections Selected                    |
| 6      | 0000                | Sections Selected                    |
| 7      | 0091                | Equipment Address                    |
| 8      | 0011                | Interrupt Lines (Micro/Macro)        |
| 9      | 0004                | Logical Unit                         |
| A      | 0018                | Total Number of Lines on Screen      |
| B      | 0001                | Number of Seconds to Wait for Output |

Skip and Backspace

The operator verifies that the cursor is returned to the first position of the line (carriage return). The cursor skips (→) 80 spaces and backspaces (←) 80 spaces. The space backspace sequence is repeated two times.

Line Clear

A line clear operation is entering spaces from the cursor position to the end of the line in display memory. Cursor reset is moving the cursor to the first character, top line. The sequence of commands executed in this section is:

1. Reset cursor to the first position, line clear.
2. Write 20 characters on the line, reset, and line clear.

3. Write 40 characters on the line, reset, and line clear.
4. Write 60 characters on the line, reset, and line clear.
5. Write 80 characters on the line, reset, and line clear.

Screen Clear

The character S is written in every character position of the display screen. Then the screen clear function is executed. The whole screen is expected to be filled with spaces and the cursor reset.

**Section 3 — Display Data Transmission**

This test displays four patterns composed of displayable characters on the screen. Upon completion of each display, the program waits about 10 seconds for the operator to judge whether the data transmission passes his criteria.

The first pattern is displaying all 96 displayable characters on the screen and reading the data back. The characters are displayed and read three times using the following methods:

1. A/Q channel
2. ADT character mode
3. ADT word mode

The second pattern is filling every character position of the screen with the character H. The operator not only verifies that the blanking and unblanking are correct, but also that the vertical/horizontal video positioning yoke alignment is correct.

The third pattern is displaying the worst case pattern, which is \*U\*U\*U\*U ... \*U. The entire screen is filled with the worst case pattern.

The fourth pattern is a line of DELs (■), a line of Ws, and a line of hyphens (-).

#### Section 4 — Cursor Positioning Test

The program first clears the screen and resets the cursor to the first character on the top line. The cursor then traces consecutive V patterns on the screen by skipping to the right and moving down once until it reaches the bottom line, and then skipping to the right and moving up once until the top line is reached. The V patterns are repeated until the cursor comes to the rightmost column of the screen. A character (1, 2, . . . 9.0) is output in every position of the path. After the pattern is completed, the cursor is reset to the home position. Every position of the screen is read (from left to right, top to bottom) and checked against the expected pattern.

#### Section 5 — Lamp Check

LAMP CHECK is written on the CDT by the program. It then locks the keyboard so that the indicator LOCK KEYBOARD can be on. The I/O required to cause the carrier on and clear to send indicators to be on is reading the content of the cursor. The operator is to see that the KEYBOARD LOCK, character (CHAR), carrier on (C0), and clear to send (CTS) stay on for about 30 seconds while the program reads from the screen. After each I/O operation, the program validates for I/O error.

The indicators LINE, BLOCK, ALERT, and FORMAT MODE are off.

If the optional indicators for request to send (RTS), data terminal ready (DTR), receive data (REC DATA), and transmitted data (TRANS DATA) are available, these too are left for the operator to see that they stay on.

#### Section 6 — Keyboard Test

The program outputs a message instructing the operator to enter the characters 1234567890. Upon receiving the data, the program will verify that the data read in are indeed 1234567890. If incorrect, an error message that includes the received data is output.

#### Section 7 — Computer Echo Test

The operator is asked to input any alphanumeric characters from the keyboard. The program then echoes the data back on the screen. The correctness of the echo test is judged by the operator.

#### Section 8 — Keyboard Enable Enable/Disable Test

The program outputs the function STX (keyboard disable) to the LIAT. The operator is asked to input the characters LOCK, followed by pressing the break key; followed by the characters UNLOCKED. If the keyboard enable and disable functions are working properly, the program should only receive the characters UNLOCK. The ED creates lost data because the program is not reading it. The status of the LIAT is expected to reflect the lost data condition. Error messages are output if otherwise.

#### Section 9 — Parity Error Check

The operator is asked to set the PARITY EVEN/ODD switch to ODD, input one alphanumeric character from the keyboard, set the PARITY EVEN/ODD switch back to EVEN, and input one alphanumeric character. The program expects the parity bit in the status to be on while reading the first character but off when reading the second character.

#### MESSAGES

##### Action Codes

Table 7-14 lists the action codes issued by LIAT2.

#### RESTRICTIONS

There are no restrictions on this test.

TABLE 7-14. LIAT2 OUTPUT MESSAGES

| Action Code | Test Section | English Text    | Description                          | Additional Information                                                                                                                                   |
|-------------|--------------|-----------------|--------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0711        | All          | INTERNAL REJECT | Internal reject from LIAT            | DIFN = Last director function output<br>STAT = Last status of LIAT                                                                                       |
| 0721        | All          | EXTERNAL REJECT | External reject from LIAT            | DIFN = Last director function output<br>STAT = Last status of LIAT                                                                                       |
| 0731        | All          | STATUS ERR      | Status error                         | DIFN = Last director function output<br>EXST = Expected status<br>ACST = Expected status                                                                 |
| 0732        | 8            | NO LOST DATA    | Lost data expected but not there     | ACST = Actual status<br>EXST = Expected status<br>(The ED from the keyboard should cause lost data but did not.)                                         |
| 0733        | 3            | ADT ERROR       | ADT error                            | DIFN = Last director function output<br>STAT = Last status of LIAT<br>FWA = First word address of data block<br>CWA = Current word address of data block |
| 0741        | 3            | DATA ERROR      | Data read not equal to data expected | ACDA = Actual data<br>EXDA = Expected data                                                                                                               |
| 0742        | 4            | CURSOR ERROR    | Cursor error                         | None                                                                                                                                                     |
| 0750        | All          | GHOST INT       | Ghost interrupt                      | None                                                                                                                                                     |
| 0751        | All          | TIME OUT        | Time out                             | DIFN = Last director function output<br>STAT = Last status of LIAT                                                                                       |
| 0771        | 9            | NO PARITY       | Parity error expected but not found  | ACST = Actual status<br>EXST = 00A0 is the expected status                                                                                               |

# CARD READER/ LINE PRINTER ECHO TEST

## TEST IDENTIFICATION

08

## TEST NAME

CRECO

## PURPOSE

The card reader/line printer echo test (CRECO) tests the card reader/line printer controller in an echo mode using the hardware test mode capability. This means that the actual equipment need not be physically attached, as only the board is tested.

## PARAMETERS

Table 7-15 lists the run parameters used for the CRECO tests. Parameter C of the list contains the character that is output and read during operations 3 and four of section 1. This character may be changed to test different data patterns. Parameter D of the list specifies the parity mode of the line printer and must be set to match the hardware parity selection of odd or even.

## OVERLAYS

No overlays are needed for the overlay version.

## ORGANIZATION

CRECO consists of an initialization section, four test sections with from one to seven subsections, and a termination section. Tables 7-16, 7-17, 7-18, and

TABLE 7-15. CRECO RUN PARAMETERS

| Word   | Initial Value (Hex) | Definition                                                              |
|--------|---------------------|-------------------------------------------------------------------------|
| TESTID | 0008                | Test ID                                                                 |
| PASCNT | 0000                | Pass Count                                                              |
| ERRCNT | 0000                | Error Count                                                             |
| 1      | 2080                | Control Word                                                            |
| 2      | 0001                | Repeat Count                                                            |
| 3      | 1234                | Sections Selected                                                       |
| 4      | 0000                | Sections Selected                                                       |
| 5      | 0000                | Sections Selected                                                       |
| 6      | 0000                | Sections Selected                                                       |
| 7      | 0580                | Card Reader Equipment Code                                              |
| 8      | 00BB                | Card Reader Interrupt Line Micro/Macro                                  |
| 9      | 0000                | Logical Unit                                                            |
| A      | 0200                | Line Printer Equipment Code                                             |
| B      | 0044                | Line Printer Interrupt Line Micro/Macro                                 |
| C      | 0055                | Output Data Character for operations 3 and 4 of section 1               |
| D      | 0001                | Line Printer Parity Mode Selection<br>0 = Even parity<br>1 = Odd parity |

7-19 show the relationships between the operations directed at the controller and the expected status and data that result. The four tables correspond to the four sections. The operation corresponds to the subsection numbers.

## Initialization Section

The initialization section reads and informs the operator of the card reader and line printer protect status. The protect status is ignored in sections 1 through 4.

TABLE 7-16. TEST SECTION 1 CRECOI

| Sub-section | Operation                                                                  | Card Reader Function | Line Printer Function | Card Reader Status                                                             | DIR Status 1 | DIR Status 2 | Line Printer Status                                                       |                  |
|-------------|----------------------------------------------------------------------------|----------------------|-----------------------|--------------------------------------------------------------------------------|--------------|--------------|---------------------------------------------------------------------------|------------------|
| 1           | CLEAR/SET TEST MODE                                                        |                      |                       | READY                                                                          | \$1          | 0            | READY<br>EOP<br>DATA (indefinite)                                         | \$11<br>or<br>19 |
| 2           | CR FEED<br>A/Q MODE<br>LP-DATA INT.<br>CR-ALL INTS.                        | \$9C                 | \$4                   | READY BUSY                                                                     | \$3          | 0            | READY<br>INTERRUPT<br>DATA<br>EOP<br>LOAD IMAGE<br>PAPER OUT<br>BUFFER OV | \$D1D            |
| 3           | LP DATA OUTPUT<br>A/Q MODE<br>LP-NO INTS<br>CR-DATA INT<br>DATA FROM P. L. | \$4                  | \$2                   | READY<br>BUSY<br>INTERRUPT<br>DATA                                             | \$F          | 0            | READY<br>DATA<br>EOP<br>LOAD IMAGE<br>PAPER OUT<br>BUFFER OV              | \$D19            |
| 4           | CR DATA INPUT<br>A/Q MODE<br>CR NO INT<br>LP NO INT                        | \$2                  | \$2                   | READY<br>BUSY<br>+<br>DATA<br>CHECK                                            | \$3          | 0            | READY<br>DATA<br>EOP<br>LOAD IMAGE<br>PAPER OUT<br>BUFFER OV              | \$D19.           |
| 5           | ADT TRANSFER<br>ADT MODE<br>CR ALARM INT                                   | \$D0                 | \$40                  | INTERRUPT<br>DATA<br>ALARM<br>LOST DATA<br>NOT READY<br>ADT MODE<br>DATA CHECK | \$66C        | 0            | READY<br>EOP<br>ADT MODE                                                  | \$211            |

**Section 1 — Data Path Check**

Section 1 functions the devices and then reads the status back. The data paths of the line printer and the card reader are checked and the status sent back to the operator. Table 7-16 lists the operations required for data path checking. Subsection 5 of section 1 tests the ability of the hardware to transfer data in ADT mode using the following data:

1, 2, 4, 8, \$10, \$20, \$40, \$80,  
\$80, \$40, \$20, \$10, 8, 4, 2, 1,  
\$FF, \$FE, \$FD, \$FB, \$F7, \$EF,  
\$DF, \$BF, \$7F, \$7E, \$7C, \$78,  
\$70, \$60, \$40, 0

The A/Q response and interrupt signals are also checked.

TABLE 7-17. TEST SECTION 2 CRECO2

| Sub-section | Operation                                               | Card Reader Function | Line Printer Function | Card Reader Status                 | DIR Status 1 | DIR Status 2 | Line Printer Status                                                       |                    |
|-------------|---------------------------------------------------------|----------------------|-----------------------|------------------------------------|--------------|--------------|---------------------------------------------------------------------------|--------------------|
| 1           | CLEAR/SET TEST MODE                                     |                      |                       | READY                              | \$1          | 0            | READY<br>EOP<br>DATA (indefinite)                                         | \$11<br>or<br>\$19 |
| 2           | CR FEED<br>A/Q MODE<br>LP DATA INT<br>CR NO INT         | \$80                 | \$4                   | READY<br>BUSY                      | \$3          | 0            | READY<br>INTERRUPT<br>DATA<br>EOP<br>LOAD IMAGE<br>PAPER OUT<br>BUFFER OV | \$D1D              |
| 3           | LP DATA OUTPUT<br>A/Q MODE<br>LP DATA INT<br>CR NO INT  | \$2                  | \$4                   | READY<br>BUSY<br>DATA              | \$B          | 0            | READY<br>INTERRUPT<br>DATA<br>EOP<br>LOAD IMAGE<br>PAPER OUT<br>BUFFER OV | \$D1D              |
| 4           | LP DATA OUTPUT<br>A/Q MODE<br>LP NO INT<br>CR ALARM INT | \$10                 | \$2                   | READY<br>BUSY<br>INTERRUPT<br>DATA | \$6F         | 0            | READY<br>DATA<br>EOP<br>LOAD IMAGE<br>PAPER OUT<br>BUFFER OV              | \$D19              |

TABLE 7-18. TEST SECTION 3 CRECO3

| Sub-section | Operation                                       | Card Reader Function | Line Printer Function | Card Reader Status | DIR Status 1 | DIR Status 2 | Line Printer Status                                                       |                    |
|-------------|-------------------------------------------------|----------------------|-----------------------|--------------------|--------------|--------------|---------------------------------------------------------------------------|--------------------|
| 1           | CLEAR/SET TEST MODE                             |                      |                       | READY              | \$1          | 0            | READY<br>EOP<br>DATA (indefinite)                                         | \$11<br>or<br>\$19 |
| 2           | CR FEED<br>A/Q MODE<br>LP DATA INT<br>CR NO INT | \$80                 | \$4                   | READY              | \$3          | 0            | READY<br>INTERRUPT<br>DATA<br>EOP<br>LOAD IMAGE<br>PAPER OUT<br>BUFFER OV | \$D1D              |

TABLE 7-18. TEST SECTION 3 CRECO3 (Continued)

| Sub-section | Operation                                         | Card Reader Function | Line Printer Function | Card Reader Status                                                           | DIR Status 1 | DIR Status 2 | Line Printer Status                                                       |       |
|-------------|---------------------------------------------------|----------------------|-----------------------|------------------------------------------------------------------------------|--------------|--------------|---------------------------------------------------------------------------|-------|
| 3           | CR FEED<br>A/Q MODE<br>LP DATA INT<br>CR NO INT   | \$80                 | \$4                   | READY<br>BUSY                                                                | \$3          | 0            | READY<br>INTERRUPT<br>DATA<br>EOP<br>LOAD IMAGE<br>PAPER OUT<br>BUFFER OV | \$D1D |
| 4           | LP DATA OUT<br>A/Q MODE<br>LP NO INT<br>CR NO INT | \$2                  | \$2                   | READY<br>BUSY<br>HOPPER EMPTY<br>STACKER FULL<br>FEED ERROR<br>STACKER ERROR | \$3          | \$27         | READY<br>EOP<br>LOAD IMAGE<br>PAPER OUT<br>BUFFER OV                      | \$D11 |
| 5           | LP DATA OUT<br>A/O MODE<br>CR NO INT<br>LP NO INT | \$2                  | \$2                   | NOT CHECKED                                                                  |              |              | REJECT                                                                    |       |

TABLE 7-19. TEST SECTION 4 CRECO4

| Sub-section | Operation                                       | Card Reader Function | Line Printer Function | Card Reader Status              | DIR Status 1 | DIR Status 2 | Line Printer Status                                                       |                    |
|-------------|-------------------------------------------------|----------------------|-----------------------|---------------------------------|--------------|--------------|---------------------------------------------------------------------------|--------------------|
| 1           | CLEAR/SET TEST<br>MODE                          |                      |                       | READY                           | \$1          | 0            | READY<br>EOP<br>DATA<br>(indefinite)                                      | \$11<br>or<br>\$19 |
| 2           | CR FEED<br>A/Q MODE<br>LP DATA INT<br>CR NO INT | \$80                 | \$4                   | READY<br>BUSY                   | \$3          | 0            | READY<br>INTERRUPT<br>DATA<br>EOP<br>LOAD IMAGE<br>PAPER OUT<br>BUFFER OV | \$D1D              |
| 3           | CR DATA IN<br>A/Q MODE<br>NO INTS               | \$2                  | \$2                   | REJECT                          |              |              | NOT CHECKED                                                               |                    |
| 4           | LP PRINT<br>A/Q<br>CR ALARM INT<br>LP NO INT    | \$10                 | \$22                  | INTERRUPT<br>ALARM<br>NOT READY | \$224        | 0            | READY<br>DATA<br>EOP                                                      | \$19               |

TABLE 7-19. TEST SECTION 4 CRECO4 (Continued)

| Sub-section | Operation                                          | Card Reader Function               | Line Printer Function    | Card Reader Status | DIR Status 1 | DIR Status 2 | Line Printer Status                         |      |
|-------------|----------------------------------------------------|------------------------------------|--------------------------|--------------------|--------------|--------------|---------------------------------------------|------|
| 5           | CR ILLEGAL<br>FUNCT<br>LP NO INT                   | \$4<br>\$8<br>\$10<br>\$40<br>\$80 | \$0<br>NO<br>OUT-<br>PUT | REJECT             |              |              | NOT CHECKED                                 |      |
| 6           | LP CLEAR<br>CR NO INT<br>LP CLEAR,<br>ALARM<br>INT | \$2                                | \$11                     | READY<br>EOP       | \$11         | 0            | READY<br>INTERRUPT<br>EOP<br>ALARM<br>ERROR | \$75 |
| 7           | LP PRINT<br>CR NO INT                              | \$2                                | \$20                     | NOT CHECKED        |              |              | REJECT                                      |      |

**Section 2 — Card Reader Lost Data and Alarm Checking**

Section 2 forces a card reader lost data and alarm condition to occur and then reads the status back and checks it. The A/Q response and interrupt signals are also checked. Table 7-17 lists the operations required for lost data and alarm checking.

**Section 3 — Card Reader Data Lockout Checking**

Section 3 causes a card reader data lockout to occur (i. e., second feed function causes data on first card to be ignored). The A/Q response and interrupt signals are also checked. Table 7-18 lists the operations required for card reader data lockout checking.

**Section 4 — Line Printer and Simulated Card Reader/ Line Printer Alarm Condition Checking**

Section 4 causes a simulated alarm condition to occur on the card reader and the line printer. Section 4 also

checks the line printer control function status. The A/Q response and interrupt signals are also checked. Table 7-19 lists the operations required for section 4.

**MESSAGES**

**Action Codes**

Table 7-20 lists the CRECO action codes.

**RESTRICTIONS**

The CRECO test has no restrictions.

TABLE 7-20. CRECO OUTPUT MESSAGES

| Action Code | Test Section | English Text      | Description                | Additional Information                                                                           |
|-------------|--------------|-------------------|----------------------------|--------------------------------------------------------------------------------------------------|
| 0810        | All          | NO CR REJECT      | No reject on input         | None                                                                                             |
| 0811        | All          | CR FUNCTION REJT  | Internal reject on input   | None                                                                                             |
| 0812        | All          | CR DATA IN REJT   | External reject on input   | None                                                                                             |
| 0820        | All          | NO LP REJECT      | No reject on output        | None                                                                                             |
| 0821        | All          | LP FUNCTION REJT  | Internal reject on output  | None                                                                                             |
| 0822        | All          | LP DATA OUT REJT  | External reject on output  | None                                                                                             |
| 0831        | All          | CR STATUS REJT    | Card reader status error   | ECR1/2 = Expected card reader status<br>1 and 2<br>ACR1/2 = Actual card reader status<br>1 and 2 |
| 0832        | All          | LP STATUS REJT    | Line printer status error. | ELPS = Expected line printer status<br>ALPS = Actual line printer status                         |
| 0841        | All          | DATA/STATUS ERROR | Data error                 | EDAT = Expected data<br>ADAT = Actual data                                                       |
| 0851        | All          | NO INTERRUPT      | No macro interrupt         | None                                                                                             |
| 0853        | All          | GHOST INTERRUPT   | Unexpected interrupt       | None                                                                                             |

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The level II program consists of a core-resident monitor and level II diagnostic tests. The level II diagnostic tests execute under control of the monitor.

The level II diagnostic tests are:

- CR104 — Card reader tests
- CRUT1 — Card reader utility test
- CRUT2 — Card reader utility test
- LP408 — Line printer tests
- LCTTA — Tape transport controller tests
- LCTTB — Tape transport and controller tests
- CLA2A — Dual channel communication line adapter tests

In addition to the above tests, four multiplexing tests run under control of the monitor.

- C104M
- L408M
- LCTTM
- CLA2M

See the Multiplexing Tests section (section 9) for further information.

# CARD READER TEST

## TEST IDENTIFICATION

11

## TEST NAME

CR104

## PURPOSE

The purpose of this test is to detect, isolate, and note all detectable error conditions not covered by the test mode program or utility packages CRUT1 and CRUT2 for the card reader/line printer controller and card reader.

## PARAMETERS

Parameter display and modification are handled by the monitor. Initial values for the card reader parameters are illustrated in table 8-1.

## OVERLAYS

Two overlays are used in the overlay version:

| Overlay | Test Sections Tested |
|---------|----------------------|
| 1       | 0-3                  |
| 2       | 4-5                  |

## ORGANIZATION

The card reader diagnostic consists of an initialization section and five test sections.

### Initialization Section

This section configures the micro and macro interrupt lines for the card reader. The diagnostic logical unit

TABLE 8-1. CR104 RUN PARAMETER LIST

| Word   | Initial Value (Hex) | Definition                                     |
|--------|---------------------|------------------------------------------------|
| TESTID | 0011                | Test ID                                        |
| PASCNT | 0000                | Pass Count                                     |
| ERRCNT | 0000                | Error Count                                    |
| 1      | 2080                | Control Word                                   |
| 2      | 0001                | Repeat Count                                   |
| 3      | 1234                | Sections Selected                              |
| 4      | 5000                | Sections Selected                              |
| 5      | 0000                | Sections Selected                              |
| 6      | 0000                | Sections Selected                              |
| 7      | 05BD                | Equipment Address                              |
| 8      | 00BB                | Interrupt Lines (Micro/Macro)                  |
| 9      | 0005                | Logical Unit                                   |
| A      | 3                   | Number of Cards to Read in Burst Mode 3-6      |
| B      | 2                   | Number of Seconds Delay between Bursting Cards |

is defined in the physical device table (PDT) for the card reader kernel. The ghost interrupt count is also cleared by this section. This count is checked at the end of each section.

### Section 1 — Card Reader Equipment Number Verification

This section verifies that the card reader equipment code to be used is unique to this card reader. This is accomplished by interrogation of the READY status. After first establishing the existing READY status, the test's READY status is changed by the operator. After the change is verified, the status returns to its original state and is again verified. If no change of READY is detected, an error is reported. If the card reader is not ready at this point, the operator is requested to make the device ready.

**Section 2 — Status Verification**

This section verifies the existence of the proper status conditions for hopper empty and stacker full. Data cards are not read during this section.

A request is made to make the hopper empty and the stacker full. The operator is given 30 seconds to response. The alarm, hopper empty, and stacker full status bits should be present. After verifying this status, a request is issued to make the card reader hopper not empty and stacker not full. The hopper and stacker status bits are examined to verify this condition.

Ghost interrupts are reported at the end of the section.

**Section 3 — I/O Data Input**

This section reads a test deck until an end-of-deck (EOD) indicator is read. The EOD card has all 12 channels punched in columns 1 and 2 and the remaining 78 columns are blank (see figure 8-1). The test deck checks for rejects and verifies that data status bits and EOP are present while being interrupt driven. All necessary status conditions are monitored. The card data for this section is illustrated in figure 8-2. The input cards are monitored for data errors and all columns in error for any card read are reported.

All data errors per card are displayed by the informative message on the CDT as follows (printed only if data errors found):

| ROW NO. | 12 | 11 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | TOTAL ERROR | COL ERROR |
|---------|----|----|---|---|---|---|---|---|---|---|---|---|-------------|-----------|
| ERROR   | 1  |    |   |   |   |   |   | 0 |   |   |   | 0 |             |           |

Where: Blank is no error found for 80 columns.  
 1 is one column not punched but read as being punched.  
 0 is one column punched but read as not being punched.

TOTAL ERROR is the current accumulative error count from the beginning of the test deck. All nondata errors are reported as secondary errors.

COL is the column error occurred in.

Ghost interrupts are reported at the end of the section.

**Section 4 — Card Slippage Test**

Card slippage is checked for in this section. Section 4 is identical to section 3 except that the card input data is different. The card data for this section is illustrated in figure 8-3. The EOD card terminates the deck.

**Section 5 — Burst Input Test**

This section follows the procedure given for section 3 except that the data cards are read in a cycle determined by the operator. The number of cards to be read is determined by run parameter A. The delay between cycles is determined by run parameter B. The resulting operations of this section are:

Read Cards (Burst)

The number of cards is set in run parameter A. The value must be greater than 2 and less than 7.

Delay (After Each Burst)

The number of seconds (length of delay) is set in run parameter B. The value is zero to 7FFF (32K<sub>10</sub>).

Repeat (After the Burst and Delay)

The cycle is repeated starting at the reading of cards and continuing until the EOD card is read.





TABLE 8-2. CR104 OUTPUT MESSAGES

| Action Code | Test Section | English Text            | Description                                    | Additional Information                                                                                                                                                                                                                                                               |
|-------------|--------------|-------------------------|------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1111        | 1-5          | INTERNAL REJECT         | Controller did not respond to a status read.   | None                                                                                                                                                                                                                                                                                 |
| 1121        | 1            | EXTERNAL REJECT         | Controller rejected a status read.             | None                                                                                                                                                                                                                                                                                 |
| 1123        | 2-5          | EXTERNAL REJECT         | Controller rejected a status read.             | None                                                                                                                                                                                                                                                                                 |
| 1131        | 1-5          | GHOST INTERRUPT         | Interrupt with no status indications.          | STA1 = Director status 1<br>STA2 = Director status 2<br>NO = Number of interrupts                                                                                                                                                                                                    |
| 1132        | 3-5          | STACKER FULL            | Alarm — Stacker full                           | EXS1 = Expected status 1<br>STA1 = Actual status 1<br>BDST = Bits set, bits wrong with status 1<br>EXS2 = Expected status 2<br>BDBT = Bits set, bits wrong with status 2<br>TYPE = 0 Time-out status<br>= 1 Initiator status<br>= 2 Continuator status<br>COL = Card column in error |
| 1134        | 3-5          | LOST DATA               | Alarm — Lost data                              | See code 1132                                                                                                                                                                                                                                                                        |
| 1135        | 3-5          | FAIL TO FEED            | Alarm — Fail to feed                           | See code 1132                                                                                                                                                                                                                                                                        |
| 1136        | 3-5          | STACKER AREA JAM        | Alarm — Stacker area jam                       | See code 1132                                                                                                                                                                                                                                                                        |
| 1137        | 3-5          | HOPPER EMPTY            | Alarm — Hopper empty                           | See code 1132                                                                                                                                                                                                                                                                        |
| 1138        | 3-5          | READ CHECK ERR<br>ERROR | Alarm — Read check error                       | See code 1132                                                                                                                                                                                                                                                                        |
| 1139        | 2-5          | C.R. NOT READY          | Not ready                                      | See code 1132                                                                                                                                                                                                                                                                        |
| 113A        | 2-5          | ALARM                   | Alarm                                          | See code 1132                                                                                                                                                                                                                                                                        |
| 113B        | 3-5          | PREMATURE EOP           | Premature EOP — EOP before column 80           | See code 1132                                                                                                                                                                                                                                                                        |
| 113C        | 3-5          | CARD READER BUSY        | Unit busy — Occurs at time of EOP              | See code 1132                                                                                                                                                                                                                                                                        |
| 113D        | 3-5          | C.R. NOT BUSY           | Unit not busy -- Occurs during data interrupts | See code 1132                                                                                                                                                                                                                                                                        |

TABLE 8-2. CR104 OUTPUT MESSAGES (Continued)

| Action Code | Test Section | English Text  | Description                                               | Additional Information                                                                     |
|-------------|--------------|---------------|-----------------------------------------------------------|--------------------------------------------------------------------------------------------|
| 1146        | 3-5          | TIME OUT      | Time-out conditions did not interrupt.                    | See code 1132                                                                              |
| 1150        | 1            | STATUS ERROR  | On- to off-line did not change ready status.              | None<br>EXST = Expected status<br>BDST = Bits set, bits wrong with status<br>STAT = Status |
| 1160        | 3-5          | CARD SLIPPAGE | Card slippage (more than 80 data interrupts)              | See code 1132                                                                              |
| 1162        | 3-5          | DATA ERROR    | Data error — Display card count, actual and expected data | None                                                                                       |

# CARD READER CALIBRATION UTILITY

## TEST IDENTIFICATION

16

### TEST NAME

CRUT1

### PURPOSE

The purpose of this test is to detect, isolate, and note detectable error conditions during calibration testing of the card reader.

### PARAMETERS

Initial values for the parameters are illustrated in table 8-3.

### OVERLAYS

No overlays are needed for the overlay system.

### ORGANIZATION

The card reader calibration test consists of two test sections plus an initialization section.

#### Initialization Section

This section configures the micro and macro interrupt lines for the card reader. The diagnostic logical unit is defined in the physical device table (PDT) for the card reader kernel. The ghost interrupt count is also cleared by this section. This count is checked at the end of each section.

## Section 1 — Sync Calibration

This section and section 2 aid the customer engineer in performing reasonable calibrations on the card reader. Figure 8-4 shows the format of the card used

TABLE 8-3. CRUT1 RUN PARAMETER LIST

| Word   | Initial Value (Hex) | Definition                    |
|--------|---------------------|-------------------------------|
| TESTID | 0016                | Test ID                       |
| PASCNT | 0000                | Pass Count                    |
| ERRCNT | 0000                | Error Count                   |
| 1      | 0580                | Control Word                  |
| 2      | 0001                | Repeat Count                  |
| 3      | 1200                | Sections Selected             |
| 4      | 0000                | Sections Selected             |
| 5      | 0000                | Sections Selected             |
| 6      | 0000                | Sections Selected             |
| 7      | 05BD                | Equipment Address             |
| 8      | 00BB                | Interrupt Lines (Micro/Macro) |
| 9      | 0005                | Logical Unit                  |

for the sync test. This deck is identified by a different part number than the rest of the test deck. The extreme row positions, channels 12 and 9, are punched in columns 1 and 80 of the card. Cards are read until the hopper is empty or until the repeat subsection bit in the control word is not selected. This section is repeated after all the sections of the test have been run.

All data errors per card are displayed by the informative message on the CDT as follows (printed only if data errors found):

|         |    |    |   |   |   |   |   |   |   |   |   |   |       |     |
|---------|----|----|---|---|---|---|---|---|---|---|---|---|-------|-----|
| ROW NO. | 12 | 11 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | TOTAL | COL |
|         |    |    |   |   |   |   |   |   |   |   |   |   | ERROR |     |
| ERROR   | 1  |    |   |   |   |   |   | 0 | 0 |   |   |   |       |     |

Where: Blank is no error found for 80 columns.

1 is one column not punched but read as being punched.

0 is one column punched but read as not being punched.

TOTAL ERROR reflects the current accumulative error count from the beginning of the test deck. All non-data errors are reported as secondary errors.

COL indicates column error occurred in.

This section reads only one card. If more than one card is to be read, the repeat section or subsection bit in the control word must be set.

**Section 2 — Read Adjustment Calibration**

This section is identical to section 1 except for the card deck and the fact that only the first bad column is reported for errors. The column number with the error is also listed.

Figure 8-5 shows the format of the card used to make read slippage adjustments. Each card consists of a checkboard format.

**MESSAGES**

**Action Codes**

The action codes for the CRUT1 tests are listed in table 8-4.

**Action Messages**

All messages used within the section are of a directive, informative, or error nature for the operator. They are by section:

Section 1: LOAD SYNC ADJUSTMENT DECK

Section 2: LOAD READ ADJUSTMENT DECK

Section 1, 2: ROW NO. 12 11 0 1 2 3 4 5 6 7 8 9  
TOTAL ERROR COL ERROR

**RESTRICTIONS**

The card reader test cannot be run currently with the card reader and line printer echo mode test CRECO, with the card reader diagnostic CR104, or with the card reader utility program CRUT2.



TABLE 8-4. CRUT1 OUTPUT MESSAGES

| Action Code | Test Section | English Text            | Description                                   | Additional Information                                                                                                                                                                                                                                                               |
|-------------|--------------|-------------------------|-----------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1611        | 1-2          | INTERNAL REJECT         | Controller did not respond to a status read.  | None                                                                                                                                                                                                                                                                                 |
| 1623        | 1-2          | EXTERNAL REJECT         | Controller rejected a status read.            | None                                                                                                                                                                                                                                                                                 |
| 1631        | 1-2          | GHOST INTERRUPT         | Interrupt with no status indications          | STA1 = Director status 1<br>STA2 = Director status 2<br>NO = Number of interrupts                                                                                                                                                                                                    |
| 1632        | 1-2          | STACKER FULL            | Alarm — Stacker full                          | EXS1 = Expected status 1<br>STA1 = Actual status 1<br>BDST = Bits set, bits wrong with status 1<br>EXS2 = Expected status 2<br>BDBT = Bits set, bits wrong with status 2<br>TYPE = 0 Time out status<br>= 1 Initiator status<br>= 2 Continuator status<br>COL = Card column in error |
| 1634        | 1-2          | LOST DATA               | Alarm — Lost data                             | See code 1632                                                                                                                                                                                                                                                                        |
| 1635        | 1-2          | FAIL TO FEED            | Alarm — Fail to feed                          | See code 1632                                                                                                                                                                                                                                                                        |
| 1636        | 1-2          | STACKER AREA JAM        | Alarm — Stacker area jam                      | See code 1632                                                                                                                                                                                                                                                                        |
| 1637        | 1-2          | HOPPER EMPTY            | Alarm — Hopper empty                          | See code 1632                                                                                                                                                                                                                                                                        |
| 1638        | 1-2          | READ CHECK ERR<br>ERROR | Alarm — Read check error                      | See code 1632                                                                                                                                                                                                                                                                        |
| 1639        | 1-2          | C.R. NOT READY          | Not ready                                     | See code 1632                                                                                                                                                                                                                                                                        |
| 163A        | 1-2          | ALARM                   | Alarm                                         | See code 1632                                                                                                                                                                                                                                                                        |
| 163B        | 1-2          | PREMATURE EOP           | Premature EOP — EOP before column 80          | See code 1632                                                                                                                                                                                                                                                                        |
| 163C        | 1-2          | CARD READER BUSY        | Unit busy — Occurs at time of EOP             | See code 1632                                                                                                                                                                                                                                                                        |
| 163D        | 1-2          | C.R. NOT BUSY           | Unit not busy — Occurs during data interrupts | See code 1632                                                                                                                                                                                                                                                                        |
| 1646        | 1-2          | TIME OUT                | Time-out conditions did not interrupt.        | See code 1632                                                                                                                                                                                                                                                                        |

TABLE 8-4. CRUT1 OUTPUT MESSAGES (Continued)

| Action Code | Test Section | English Test  | Description                                                  | Additional Information |
|-------------|--------------|---------------|--------------------------------------------------------------|------------------------|
| 1660        | 1-2          | CARD SLIPPAGE | Card slippage (more than 80 data interrupts)                 | See code 1632          |
| 1662        | 1-2          | DATA ERROR    | Data error -- Display card count, actual and expected data / | None                   |

# CARD READER TIMING UTILITY

## TEST IDENTIFICATION

17

## TEST NAME

CRUT2

## PURPOSE

The purpose of this test is to verify the timing rates of the card reader.

## PARAMETERS

Parameter display and modification is handled by the monitor. Initial values for the parameters are shown in table 8-5.

## OVERLAYS

No overlays are needed for the overlay version.

## ORGANIZATION

The card reader diagnostic consists of one test section plus an initialization section.

### Initialization Section

This section configures the micro and macro interrupt lines for the card reader. The diagnostic logic unit is defined in the physical device table (PDT) for the card reader kernel. The ghost interrupt count is also cleared by this section. This count is checked at the end of each section.

TABLE 8-5. CRUT2 RUN PARAMETER LIST

| Word   | Initial Value (Hex) | Definition                    |
|--------|---------------------|-------------------------------|
| TESTID | 0017                | Test ID                       |
| PASCNT | 0000                | Pass Count                    |
| ERRCNT | 0000                | Error Count                   |
| 1      | 0080                | Control Word                  |
| 2      | 0001                | Repeat Count                  |
| 3      | 1000                | Sections Selected             |
| 4      | 0000                | Sections Selected             |
| 5      | 0000                | Sections Selected             |
| 6      | 0000                | Sections Selected             |
| 7      | 05BD                | Equipment Address             |
| 8      | 00BB                | Interrupt Lines (Micro/Macro) |
| 9      | 0005                | Logical Unit                  |

### Section 1 — Timing Check

This test verifies the data and card timing rates. This section should not be multiplexed with other sections. If multiplexing is enabled, the expected time may be greater than times specified. The time rates are shown in table 8-6.

A  $\pm 10\%$  tolerance is allowed. The minimum, maximum, and average card and data rates are listed at the end of the section for all items in the above table as an informative message, except the time delay for the first feed when the card reader motor is off. This rate is calculated only once.

At least four cards must be read for the informative report. Actual data is not checked in this section. Cards are read until either an EOD is encountered or until a non-data error is detected. See figures 8-6 and 8-7 for card data format. Ghost interrupts are reported at the end of the section.

TABLE 8-6. CARD READER TIME RATES

| Card Rates in Cards Per Minute (CPM)              | 300 CPM | 400 CPM | 600 CPM | 600 CPM |
|---------------------------------------------------|---------|---------|---------|---------|
| 1. Delay to first card column from a feed request |         |         |         |         |
| a. First feed request (feed motor off)            | 290 ms  | 230 ms  | 290 ms  | 230 ms  |
| b. Subsequent feed requests (feed motor off)      | 40 ms   | 30 ms   | 40 ms   | 30 ms   |
| 2. Data rates after first card column             | 0.73 ms | 0.56 ms | 0.73 ms | 0.56 ms |
| 3. Minimum card cycle time                        | 170 ms  | 165 ms  | 100 ms  | 75 ms   |

MESSAGES

Action Codes

Table 8-7 lists the CRUT2 action codes.

RESTRICTIONS

The card reader test cannot be run currently with the card reader and line printer echo mode test CRECO, with the card reader diagnostic CR104, or with the card reader utility program CRUT1.

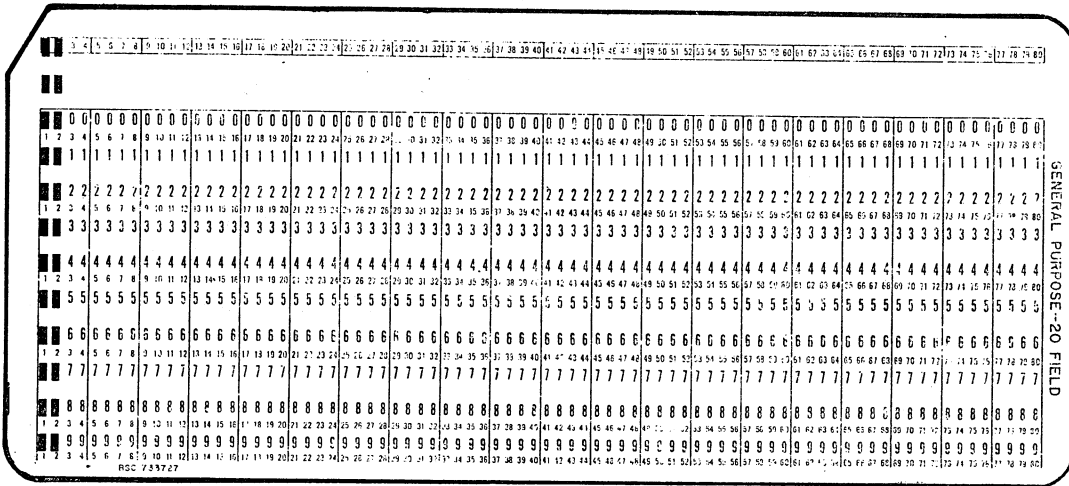


Figure 8-6. End of Deck (EOD) Card

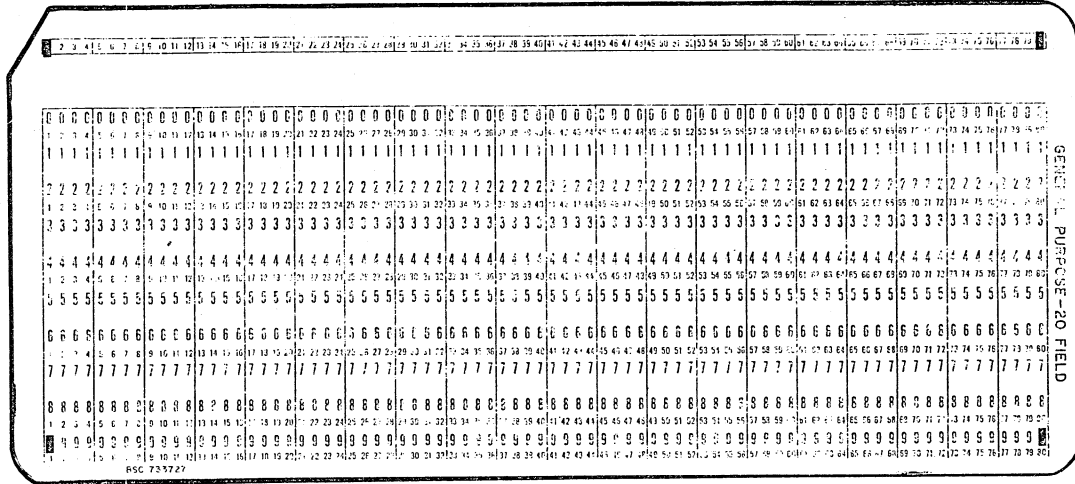


Figure 8-7. Throat Adjustment Card

TABLE 8-7. CRUT2 OUTPUT MESSAGES

| Action Code | Test Section | English Text     | Description                                  | Additional Information                                                                                                                                                                                                                                                               |
|-------------|--------------|------------------|----------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1711        | 1            | INTERNAL REJECT  | Controller did not respond to a status read. | None                                                                                                                                                                                                                                                                                 |
| 1723        | 1            | EXTERNAL REJECT  | Controller rejected a status read.           | None                                                                                                                                                                                                                                                                                 |
| 1731        | 1            | GHOST INTERRUPT  | Interrupt with no status                     | STA1 = Director status 1<br>STA2 = Director status 2<br>NO = Number of interrupts                                                                                                                                                                                                    |
| 1732        | 1            | STACKER FULL     | Alarm — Stacker full                         | EXS1 = Expected status 1<br>STA1 = Actual status 1<br>BDST = Bits set, bits wrong with status 1<br>EXS2 = Expected status 2<br>BDBT = Bits set, bits wrong with status 2<br>TYPE = 0 Time-out status<br>= 1 Initiator status<br>= 2 Continuator status<br>COL = Card column in error |
| 1734        | 1            | LOST DATA        | Alarm — Lost data                            | See code 1132                                                                                                                                                                                                                                                                        |
| 1735        | 1            | FAIL TO FEED     | Alarm — Fail to feed                         | See code 1732                                                                                                                                                                                                                                                                        |
| 1736        | 1            | STACKER AREA JAM | Alarm — Stacker area jam                     | See code 1732                                                                                                                                                                                                                                                                        |

TABLE 8-7. CRUT2 OUTPUT MESSAGES (Continued)

| Action Code | Test Section | English Text            | Description                                                     | Additional Information |
|-------------|--------------|-------------------------|-----------------------------------------------------------------|------------------------|
| 1737        | 1            | HOPPER EMPTY            | Alarm -- Hopper empty                                           | See code 1732          |
| 1738        | 1            | READ CHECK ERR<br>ERROR | Alarm -- Read check<br>error                                    | See code 1732          |
| 1739        | 1            | C.R. NOT READY          | Not ready                                                       | See code 1732          |
| 1746        | 1            | TIME OUT                | Time-out conditions<br>did not interrupt.                       | See code 1732          |
| 1760        | 1            | CARD SLIPPAGE           | Card slippage (more<br>than 80 data interrupts)                 | See code 1732          |
| 1762        | 1            | DATA ERROR              | Data error (display card<br>count, actual and<br>expected data) | None                   |
| 173A        | 1            | ALARM                   | Alarm                                                           | See code 1732          |
| 173B        | 1            | PREMATURE EOP           | Premature EOP (EOP<br>before column 80)                         | See code 1732          |
| 173C        | 1            | CARD READER BUSY        | Unit busy (occurs at<br>time of EOP)                            | See code 1732          |
| 173D        | 1            | C.R. NOT BUSY           | Unit not busy (occurs<br>during data interrupts)                | See code 1732          |

## LINE PRINTER TEST

### TEST IDENTIFICATION

12

### TEST NAME

LP408

### PURPOSE

The LP408 test is used to detect and isolate failures in the card reader/line printer controller and the line printer.

### PARAMETERS

Parameters for the line printer test follow the standard ODS parameter list structure. Device specific parameters are placed into words 7 through D of the parameter as listed in table 8-8. The 1827-30/31 printers are tested using 136 columns of data. The 1827-60 printer is tested using 132 columns of data.

### OVERLAYS

The LP408 test uses two overlays in the overlay version:

| <u>Overlay No.</u> | <u>Test Section No.</u> |
|--------------------|-------------------------|
| 1                  | 0-4                     |
| 2                  | 5-7                     |

### ORGANIZATION

The line printer test is composed of seven sections. The level II monitor is used to control the execution of the sections. Standard ODS error reporting procedures are used by this test.

TABLE 8-8. LP408 RUN PARAMETER LIST

| Word   | Initial Value (Hex) | Definition                                                                  |
|--------|---------------------|-----------------------------------------------------------------------------|
| TESTID | 0012                | Test ID                                                                     |
| PASCNT | 0000                | Pass Count                                                                  |
| ERRCNT | 0000                | Error Count                                                                 |
| 1      | 0080                | Control Word                                                                |
| 2      | 0001                | Repeat Count                                                                |
| 3      | 1234                | Sections Selected                                                           |
| 4      | 5670                | Sections Selected                                                           |
| 5      | 0000                | Sections Selected                                                           |
| 6      | 0000                | Sections Selected                                                           |
| 7      | 0201                | Equipment Address                                                           |
| 8      | 0044                | Interrupt Lines (Micro/Macro)                                               |
| 9      | 0003                | Logical Unit                                                                |
| A      | 0036                | Number of Lines for Section 4                                               |
| B      | 0188                | First and Last Print Columns for Section 6 and 7 (0184 for 1827-60 printer) |
| C      | 0045                | Character for Sections 6 and 7 (Default Code 45 is E)                       |
| D      | 0088                | Number of Columns (0084 for 1827-60 printer)                                |

### Initialization Section

This section configures the micro and macro interrupt lines for the line printer. The diagnostic logical unit is defined in the physical device table (PDT) for the line printer kernel. The ghost interrupt count is also cleared by this section. This count is checked at the end of each section. The number of characters per line is moved from the parameter list to the PDT of the driver.

### Section 1 — Validate Equipment Code

The purpose of this section is to verify that the line printer controller is responding to the correct equipment code without rejecting. Since it is necessary to be absolutely sure that the line printer controller is the one that is responding to the specified equipment

number, the program checks the READY status of the line printer while the operator is manually switching the line printer from ready to not ready and vice versa. Illegal read requests are also made to check the controller's reject logic. After the equipment code has been verified, the section checks for the correct status of the line printer after issuing a clear controller. The fourth and fifth subsections check that the card reader/line printer controller can be put into and taken out of test mode.

The subsections of section 1 are:

1. Equipment number validation
2. Illegal operation check
3. Status check
4. Test mode set check
5. Test mode clear check

### Section 2 — Line Printer Memory Test Using Rejects

This section of the line printer diagnostic tests four areas in the line printer. The four areas are:

1. Data transfers using A/Q mode
2. Hammer driver decode logic (single bit)
3. Variable length buffers (1 to 141)
4. Single bit memory test

A total of 272 lines of test data are printed on five pages of computer paper (with 57 lines per page). At the top of every page a header is printed giving column number information. The lines of data are formatted as follows:

All odd numbered lines contain the characters ABDHP and the blank repeated four times starting in column 1 for the first line. An increasing number of blanks are placed in front of the characters until line number 271 when there is only the character A printed in column 136.

All even numbered lines contain the characters blank and PHDBA repeated four times. This printout ends in column 136 for the second line and is shifted one column to the left for each successive line until on line 272 only the letter A is printed.

A typical printout is shown in figure 8-8.

### Section 3 — Forms Control Test

This section is used to verify the operation of the vertical forms control logic with the standard forms control tape. The section executes as follows:

1. Eject page and print TOP OF FORMS
2. Output four lines consisting of a single space followed by the words SINGLE SPACE
3. Output four lines consisting of a double space followed by the words DOUBLE SPACE
4. Output four lines consisting of a triple space followed by the words TRIPLE SPACE
5. Overprint the line SUPPRESS SPACE — 1234 four times so that 1 is printed once, 2 is printed twice, 3 is printed three times, and 4 is printed four times.
6. Skip to bottom of form and print BOTTOM OF FORMS.

Figure 8-9 shows an example of forms control test printout.

### Section 4 — Hammer Driver Decode Test Using Interrupts

A sliding data pattern is printed on the number of lines specified in parameter word A of the parameter list. Column number headers are printed at the top of each page. Full lines of 136-characters are used, which appear as follows:

```
@ABCDEFGH...
ABCDEFGHI...
BCDEFGHIJ...
```

Data transfers to the line printer are controlled by the data interrupt logic.

### Section 5 — Worst Case Printing Using ADT

Data is printed at the highest possible speed (300 lpm) using full buffers with alternating data characters. Because the timing of the print drum is known, it is possible to predict that a character that is 67 positions away on the print drum is in position to be printed

| <u>Line No.</u> |                         | 12345678901234567890.....1234567890123456 |
|-----------------|-------------------------|-------------------------------------------|
|                 |                         | -----                                     |
| 1               | ABDHP ABDHP ABDHP.....  |                                           |
| 2               |                         | ....HDBA PHDBA PHDBA                      |
| 3               | ABDHP ABDHP ABDHP A ... |                                           |
| 4               |                         | ...DBA PHDBA PHDBA                        |
| 5               | ABDHP ABDHP ABDHP...    |                                           |
| .               |                         | BA PHDBA PHDBA                            |
| .               | .                       | .                                         |
| .               | .                       | .                                         |
| .               | .                       | .                                         |
| .               | .                       | .                                         |
| .               | .                       | .                                         |
| .               | .                       | .                                         |
| .               | .                       | .                                         |
| .               | .                       | .                                         |
| .               | .                       | .                                         |
| .               | .                       | .                                         |
| .               | .                       | .                                         |
| .               | .                       | .                                         |
| .               | .                       | .                                         |
| .               | .                       | .                                         |
| .               | .                       | .                                         |
| .               | .                       | .                                         |
| .               | .                       | .                                         |
| .               | .                       | .                                         |
| .               | .                       | .                                         |
| .               | .                       | .                                         |
| .               | .                       | .                                         |
| .               | .                       | .                                         |
| .               | .                       | .                                         |
| .               | .                       | .                                         |
| 267             |                         | ABD                                       |
| 268             | DBA                     |                                           |
| 269             |                         | AB                                        |
| 270             | BA                      |                                           |
| 271             |                         | A                                         |
| 272             | A                       |                                           |

Figure 8-8. Line Printer Memory Test Output

immediately following the completion of the current line. Successive characters to be printed are therefore 67 characters apart.

Ten lines of characters are printed and the average print time is provided in the form of the average time required to single space and print 136 columns.†

This section prints a predefined pattern consisting of four lines of 136 columns as follows:

†Average times may vary from equipment to equipment.

The first line is filled with the character/code E/45.  
 The second line is filled with the character/code U/55.  
 The third line is filled with the character/code %/25.  
 The fourth line is filled with the character/code 5/35.

TOP OF FORM - SECTION 3  
 SINGLE SPACE  
 SINGLE SPACE  
 SINGLE SPACE  
 SINGLE SPACE  
  
 DOUBLE SPACE  
  
 DOUBLE SPACE  
  
 DOUBLE SPACE  
  
 DOUBLE SPACE  
  
 TRIPLE SPACE  
  
 TRIPLE SPACE  
  
 TRIPLE SPACE  
  
 TRIPLE SPACE  
 SUPPRESS SPACE -1234

BOTTOM OF FORM

Figure 8-9. Forms Control Test Printout

### Section 6 — Selectable Column and Pattern Utility

The purpose of this section is to allow the operator to select a set of printer columns delimited by the first and last column numbers (provided in run parameter B)

to be printed. The character used to fill this area is determined by the character code provided in run parameter C.

Ten lines of data are printed each time this section is repeated.

### Section 7 — Print Inhibit Utility Section

The purpose of this section is to allow the operator to specify a line of data characters to be output to the line printer so that he can use his scope to check the data paths in the line printer itself. Each line (from 1 to 133 characters) is terminated by a clear printer function so that no data is printed.

### MESSAGES

#### Action Codes

Table 8-9 lists the LP408 action codes.

#### Action Messages

The following action messages are used by section 1 of this test:

PRESS STOP ON LINE PRINTER WITHIN  
 30 SECONDS

PRESS START ON LINE PRINTER WITHIN  
 30 SECONDS

### RESTRICTIONS

There are no restrictions on this test.

TABLE 8-9. LP408 OUTPUT MESSAGES

| Action Code | English Text     | Description                                                                     | Additional Information                                                                              |
|-------------|------------------|---------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------|
| 1211        | INT REJ          | An internal reject occurred (section 1).                                        | INST = Initial status <sup>†</sup><br>CNST = Continuator status<br>(after interrupt)                |
| 1221        | EXT REJ          | An external reject occurred (section 1).                                        |                                                                                                     |
| 1224        | EXT REJ          | An external reject occurred.                                                    | See action code 1221.                                                                               |
| 1231        | GHOST INTERRUPT  | An unexpected interrupt occurred. The number of ghost interrupts is given.      | INST = Initial status<br>GHCT = Ghost interrupt count                                               |
| 1241        | INT REJ          | An internal reject occurred.                                                    | See action code 1221.                                                                               |
| 1244        | TIME OUT ERR     | An interrupt did not occur with the expected time. Timeout status is specified. | INST = Initial status<br>CNST = Continuator status<br>(after interrupt)<br>TOST = Timeout status    |
| 1251        | NO STATUS CHANGE | The printer status did not change as expected.                                  | INST = Initial status                                                                               |
| 1254        | ALARM/STATUS     | An alarm or other status error occurred. The bits in error are given.           | INST = Initial status<br>CNST = Continuator status<br>(after interrupt)<br>BDBT = Bad bits in error |
| 1271        | PARITY ERROR     | A parity error occurred on data transfer.                                       | See action code 1221.                                                                               |

<sup>†</sup>If either INST or CNST are equal to \$FFFF, then no status has been taken yet, or a reject occurred on status input.

# LOW-COST TAPE TRANSPORT (LCTT) CONTROLLER TEST

## TEST IDENTIFICATION

13

## TEST NAME

LCTTA

## PURPOSE

This test is used to detect and isolate failures in the low-cost tape transport controller.

## PARAMETERS

Parameters for the LCTTA tape test follow the standard ODS parameter list structure. Device specific parameters are placed into words 7 through 9 of the parameter list. Initial values for the parameters are shown in table 8-10.

## OVERLAYS

LCTTA uses one overlay in the overlay version:

| <u>Overlay No.</u> | <u>Test Section No.</u> |
|--------------------|-------------------------|
| 1                  | 0, 1, 2, 10             |

## ORGANIZATION

The magnetic tape controller is composed of two sections and 13 subsections. Both sections test the tape controller using the controller self-test features. The tape drives do not have to be connected to the controller to execute these sections.

## Section 1 — Controller Self Test (Status and Interrupt)

The LCTT controller contains a self-test capability using an internal set of micro programs. The goal of the controller test is to verify that the controller board is fully functional without the use of the tape transport.

This section verifies equipment code, interrupt ability, and setting and clearing of the status registers. Special diagnostic function codes are used for this section.

Nine subsections are used for the controller status and interrupt tests:

1. Ghost interrupt detection
2. Controller response to processor
3. Verify controller's branch micro instruction
4. Status bits can be set by micro program
5. Verify test feedback bit and conditional branch micro instruction
6. Verify the JUMP and RETURN micro instruction
7. Status bits can be cleared by micro program
8. Status bit 12 — Inoperative after execution can be set
9. Status bit 6 — Program error can be set by a number of illegal commands

## Section 2 — Controller Self Test (Counters, Timer, Data)

This section continues the testing of the controller self-test capability. Special diagnostic functions codes are used to test the controller loop counters, timer and write clock, data echo, and CRC/LRC registers.

Four subsections are used for the controller counter, timer, and data test:

1. Test the controller's internal long loop counter and related micro instructions

TABLE 8-10. LCTTA RUN PARAMETER LIST

| Word   | Initial Value (Hex) | Definition                   |
|--------|---------------------|------------------------------|
| TESTID | 0013                | Test Identification          |
| PASCNT | 0000                | Pass Count                   |
| ERRCNT | 0000                | Error Count                  |
| 1      | 2080                | Control Word                 |
| 2      | 0001                | Repeat Count                 |
| 3      | 1200                | Sections Selected            |
| 4      | 0000                | Sections Selected            |
| 5      | 0000                | Sections Selected            |
| 6      | 0000                | Sections Selected            |
| 7      | 0480                | Equipment Address            |
| 8      | 0099                | Interrupt Line (Micro/Macro) |
| 9      | 0001                | Logical Unit                 |

2. Test the controller's internal short loop counter and related micro instructions
3. Test the controller clock and clock-related micro instructions
4. Test the controller's ability to move data through its internal data registers

**MESSAGES**

**Action Codes**

Table 8-11 lists the LCTTA action codes.

**RESTRICTIONS**

The LCTTA test executes burst input in ADT mode at such a high rate of speed as to saturate the processor for a period of time. This saturation period is long

TABLE 8-11. LCTTA OUTPUT MESSAGES

| Action Code | Test Section | English Text  | Description                                                                 | Additional Information                                                                                                                                        |
|-------------|--------------|---------------|-----------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1350        | 1, 2         | UNEXP INT     | Unexpected interrupt detected                                               | STA1 = Last equipment status<br>TNCT = Ghost interrupt count                                                                                                  |
| 1380        | 1, 2         | NO INTERRUPT  | Diagnostic function failed to respond.                                      | None                                                                                                                                                          |
|             |              | CNTRL FAILURE | Diagnostic function failed.                                                 | EXST = Expected status<br>ACST = Actual status<br>EXDA = Expected data<br>ACDA = Actual data<br>ADT1 = ADT first word address<br>ADT2 = ADT last word address |
|             |              | TIME          | Controller clock out of tolerance.                                          | None                                                                                                                                                          |
| 1381        | 1            | NO RESPONSE   | First diagnostic function failed to respond. Equipment code could be wrong. | None                                                                                                                                                          |

enough to cause possible lost data conditions if operating other devices, such as the card reader, while LCTTA is executing.

The data echo and LRC/CRC diagnostic functions cannot be implemented at the macro assembly language

level. This is because the hardware read/write direction line from the controller to the processor is not being implemented. In this configuration, the macro program cannot change the direction of the transfer in time to obtain the echoed data.

# LOW-COST TAPE TRANSPORT (LCTT) CONTROLLER AND UNIT TEST

## TEST IDENTIFICATION

14

## TEST NAME

LCTTB

## PURPOSE

This test is used to detect and isolate failures in the low-cost tape transport (LCTT) controller and the LCTT drives.

## PARAMETERS

Parameters for the LCTT tape test follow the standard ODS parameter list structure. Device-specific parameters are placed into words 7 through F of the parameter list. Initial values for the parameters are shown in table 8-12.

Selection of the data patterns (words B and C of parameter table) is limited by the type of transport being tested. All data patterns (0000 through FFFF) are possible on a nine-track transport. On seven-track transports, data cannot be written from bits 15, 14, 7 or 6 (these bits must be 0), as a program error results from the controller. Data patterns for seven-track transports are limited to the range 0000 through 3F3F with bits 15, 14, 7, and 6 always being zero.

## OVERLAYS

LCTTB uses nine overlays in the overlay version:

| <u>Overlay No.</u> | <u>Test Section No.</u> |
|--------------------|-------------------------|
| 1                  | 0, 1                    |
| 2 through 8        | 2 through 8             |
| 9                  | 9 through C and 10      |

TABLE 8-12. LCTTB RUN PARAMETER LIST

| Word              | Initial Value (Hex) | Definition                                                                                                                                                                                                     |                  |                  |
|-------------------|---------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------|------------------|
| TESTID            | 0014                | Test ID                                                                                                                                                                                                        |                  |                  |
| PASCNT            | 0000                | Pass Count                                                                                                                                                                                                     |                  |                  |
| ERRCNT            | 0000                | Error Count                                                                                                                                                                                                    |                  |                  |
| 1                 | 2080                | Control Word                                                                                                                                                                                                   |                  |                  |
| 2                 | 0001                | Repeat Count                                                                                                                                                                                                   |                  |                  |
| 3                 | 1234                | Sections Selected                                                                                                                                                                                              |                  |                  |
| 4                 | 5678                | Sections Selected                                                                                                                                                                                              |                  |                  |
| 5                 | 9A00                | Sections Selected                                                                                                                                                                                              |                  |                  |
| 6                 | 0000                | Sections Selected                                                                                                                                                                                              |                  |                  |
| 7                 | 0480                | Equipment Address                                                                                                                                                                                              |                  |                  |
| 8                 | 0099                | Interrupt Line (Micro/Macro)                                                                                                                                                                                   |                  |                  |
| 9                 | 0001                | Logical Unit                                                                                                                                                                                                   |                  |                  |
| A                 | 0100 <sup>†</sup>   | Uses PDT for format Unit, Track, Density<br>Unit (0-3) — Bits 12, 13<br>Track (7, 9) — Bit 11 (1 = 7-track; 0 = 9-track)<br>Density — Bits 8, 9<br>01 = 800 bpi } QSS<br>10 = 556 bpi } Only<br>11 = 200 bpi } |                  |                  |
| B                 | 2A15                | Word 1 — Standard Data Pattern                                                                                                                                                                                 |                  |                  |
| C                 | 2A15                | Word 2 — Standard Data Pattern                                                                                                                                                                                 |                  |                  |
| D                 | 0190                | Utility Record Size (Maximum)                                                                                                                                                                                  |                  |                  |
| E                 | 0000                | Utility Transfer Direction (1 = Write)                                                                                                                                                                         |                  |                  |
| F                 | 0000                | Data Error Flag<br>0 = Track failure information based on total data transferred<br>1 = Information on bit failure for each track<br>2 = Good word, bad word information                                       |                  |                  |
| <sup>†</sup> Unit | 7 TK/<br>200 bpi    | 7 TK/<br>556 bpi                                                                                                                                                                                               | 7 TK/<br>800 bpi | 9 TK/<br>800 bpi |
| 0                 | 0B00                | 0A00                                                                                                                                                                                                           | 0900             | 0100             |
| 1                 | 1B00                | 1A00                                                                                                                                                                                                           | 1900             | 1100             |
| 2                 | 2B00                | 2A00                                                                                                                                                                                                           | 2900             | 2100             |
| 3                 | 3B00                | 3A00                                                                                                                                                                                                           | 3900             | 3100             |

## ORGANIZATION

The magnetic tape test is composed of 12 sections. Sections 1 through 8 test the tape drives as well as the controller. Sections 9 and A are standard tape creation and standard tape reading to verify drive compatibility. Section B requires manual intervention to check the not ready and write protect features. Section C is a utility test in which the data, record length, and direction of transfer are specified by the user to permit de-skewing adjustments.

The rewind function is only used in sections 9 and A (drive compatibility testing). This permits positioning the tape to any point and starting the test in the event that the tape has a defective area.

### Section 1 — Alternate Tracks and Frames Data Pattern

This section writes and reads records of a specified data pattern, and the data is checked for accuracy. Record length is 400 words, and the pattern is repeated 4,000 times. The test cycles to completion of this section saving and analyzing data bit failures unless a primary status error occurs. In this case, it reports the primary error and discontinues the pattern checking. At the completion of the section, any data errors that occurred are reported based on the number of data bit errors and the relationship of the data bit errors to other data bits. Any secondary status errors that occurred are also reported.

This test pattern writes a checkerboard pattern on the magnetic tape. The tracks and data frames are changed for each frame of data written:

|               |             |        |
|---------------|-------------|--------|
| Test Pattern: | Seven-track | 2A15   |
|               |             | REPEAT |
|               | Nine-track  | A956   |
|               |             | REPEAT |

### Section 2 — Ones and Zero Data Pattern

The description of the record length, amount of data, error analysis and error reporting for section 2 is the same as for section 1.

This test pattern writes a rolling 1 and 0 pattern across the head assembly. Each data frame is also the complement of the previous frame.

|               |             |        |
|---------------|-------------|--------|
| Test Pattern: | Seven-track | 3F00   |
|               |             | 3E01   |
|               |             | 3D02   |
|               |             | 3B04   |
|               |             | 3708   |
|               |             | 2F10   |
|               |             | 1F20   |
|               |             | REPEAT |
|               | Nine-track  | FF00   |
|               |             | F708   |
|               |             | FD02   |
|               |             | 7F80   |
|               |             | BF40   |
|               |             | CF20   |
|               |             | EF10   |
|               |             | FE01   |
|               |             | FB04   |
|               |             | REPEAT |

### Section 3 — Ones to Zeros to Ones Data Pattern

The description of the record length, amount of data, error analysis, and error reporting for section 3 is the same as for section 1.

This test pattern starts with all ones in the first frame followed by several frames of zeros. The last frame is then changed to all ones.

|               |             |        |
|---------------|-------------|--------|
| Test Pattern: | Seven-track | 3F00   |
|               |             | 0000   |
|               |             | 0000   |
|               |             | 0000   |
|               |             | 003F   |
|               |             | REPEAT |
|               | Nine-track  | FF00   |
|               |             | 0000   |
|               |             | 0000   |
|               |             | 0000   |
|               |             | 00FF   |
|               |             | REPEAT |

#### Section 4 — Zeros to Ones to Zeros Data Pattern

The description of the record length, amount of data, error analysis, and error reporting for section 4 is the same as for section 1.

This test pattern starts with all zeros in the first frame followed by several frames of ones. The last frame is then changed to all zeros.

|               |             |                                                |
|---------------|-------------|------------------------------------------------|
| Test Pattern: | Seven-track | 003F<br>3F3F<br>3F3F<br>3F3F<br>3F00<br>REPEAT |
|               | Nine-track  | 00FF<br>FFFF<br>FFFF<br>FFFF<br>FF00<br>REPEAT |

#### Section 5 — Parity Testing Pattern

The description of the record length, amount of data, error analysis, and error reporting for section 5 is the same as for section 1.

This section tests the parity generating and monitoring logic using worse case parity generating patterns. Patterns are used that change the state of the parity bit and data track for each frame. In addition, seven-track tests are run using both odd and even parity.

|               |             |                |
|---------------|-------------|----------------|
| Test Pattern: | Seven-track | 2A2D<br>REPEAT |
|               | Nine-track  | A976<br>REPEAT |

A subsection of this section reads data in the opposite parity than it was written in to generate and test the ability to detect parity errors for seven-track units.

#### Section 6 — Start/Stop Testing

This section verifies the start stop timing of the LCTT drive by writing and reading variable length records. The variable records are written completely on tape before the data is read. The data is equal to the record

size except for the file marks. The pattern of 10 variable records is written 20 times. The tape is then backspaced and the records read and the data checked.

The record lengths are as follows:

FILE MARK, FILE MARK, FILE MARK, FILE  
MARK, FILE MARK, 9, 20, 40, 80,  
(repeated 20 times)

#### Section 7 — Erase Head Testing

This section verifies that the erase head is capable of erasing by the overwriting of complementary data and by the use of the erase function. This section consists of three subsections:

1. All ones are written on the same physical length of tape five times. All zeros are then written once. The record is then read and the data checked.
2. All zeros are written on the same physical length of tape five times. All ones are then written once. The record is then read and the data checked.
3. Two records of different data are written in sequence. A backspace is performed and an erase function is performed. Another backspace is performed and the record is read and the data checked to verify that the first record was read.

#### Section 8 — Tape Positioning / File Mark Test

This section verifies forward and reverse tape positioning and file mark recognition and positioning. This is done in two subsections:

1. A group of 60 variable-length records are written on tape. The data is the sequence number of the record. Sixty backspaces are performed and the data checked for correct position. Fifty-eight reads followed by a read and check data are performed to verify the last record. This procedure is repeated for 50, 40, 30, 20, and 10 backspaces from the last record.

The record length of the group is 400, 9, 50, 400, 30, 100, 15, 300, 10, and 200, repeated six times.

2. A sentinel record is written followed by 50 file marks followed by a sentinel record. Fifty-two backspaces are performed, verifying that the file mark does not set. The initial sentry record is read and checked. Fifty reads are performed checking for a file mark indication. The last entry record is read and verified.

### Section 9 — Creation of Standard Tape for Drive Compatibility

This section together with Section A ensures that tapes written on one drive can be read on another drive. The configuration requires that two drives of the same model are available.

A pattern prestored in the parameter table is used. The tape is first rewound and the selected pattern is written in 100 records of 400 words each record. The tape can then be dismounted and mounted on another drive. Section A can then be executed to read the tape and check the data.

### Section A — Read and Check Standard Tape

This section reads tape written in section 9. Data is read and checked against the selected pattern specified in the parameter table.

If data errors are encountered the data error is reported along with the good and bad data word.

### Section B — Status Verification

This section verifies the existence of the proper status conditions for the following:

1. Drive not ready
2. Write ring removed
3. Timeout

### Section C — Utility for Adjustments

This section provides utilities to permit read or write operations to allow transport de-skewing adjustments. The operator is able to specify a data pattern consisting of two computer words (parameters B and C) and record size (parameter D) in the range of 9-400 word records. No data checking or error reporting is done. The direction of the data transfer is controlled by parameter word E (1 = write, 0 = read).

### MESSAGES

#### Action Codes

Table 8-13 lists the LCTTB action codes.

#### Action Messages

ACTION requests to operator occur in section 11 and are as follows:

REMOVE WRITE RING AND MAKE UNIT  
READY WITHIN 180 SECONDS

INSERT WRITE RING AND MAKE UNIT READY  
WITHIN 180 SECONDS

### RESTRICTIONS

There are no restrictions on this test.

TABLE 8-13. LCTTB ACTION CODES

| Action Code | Test Section | English Text                   | Description                                                                                         | Additional Information†                                                                                                                                      |
|-------------|--------------|--------------------------------|-----------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1430        | 1-8          | MOTION FAILURE                 | Error while executing a function to selected unit                                                   | STIN = Initiator status<br>STCN = Continuator status<br>FLCD= Fault code<br>0 = Timeout<br>2 = Continuator error<br>3 = Parity error<br>14 = Initiator error |
|             |              | INOP ON SELECT<br>INOP ON EXEC | Inoperative on selection<br>Inoperative on execution                                                |                                                                                                                                                              |
| 1431        | 1-8          | DATA + STATUS ERR              | Track failure cannot be isolated and status failure errors as well as data errors occurred.         | TK1 through TK8 = Count of failures that track<br>STA1 = Last equipment status<br>EXDA = Expected data<br>ACDA = Actual data                                 |
| 1432        | 1-8          | STATUS BIT                     | Status bits 10 (dropout) or bit 13 (data error) set                                                 | BT10 = Count of bit 10 failures<br>BT13 = Count of bit 13 failures                                                                                           |
|             | 6-8          | STATUS ERROR                   | Status bit 10 (dropout) or bit 13 (data error) set                                                  | STA1 = Last equipment status<br>EXDA = Expected data<br>ACDA = Actual data                                                                                   |
| 1433        | 1-B          | TIMEOUT BIT SET                | Status bit 9 set, timeout                                                                           | See action code 1430.                                                                                                                                        |
| 1434        | 1-B          | INOP ON SELECT                 | Status bit 0 set, inoperative on selection                                                          | See action code 1430.                                                                                                                                        |
| 1435        | 1-B          | WRITE LOCKOUT                  | Status bit 4 set, write lockout                                                                     | See action code 1430.                                                                                                                                        |
| 1436        | 1-B          | END OF TAPE                    | Status bit 15 set, end of tape                                                                      | See action code 1430.                                                                                                                                        |
| 1437        | 1-B          | READ AFTER WRITE               | Status bit 3, read after write is set                                                               | See action code 1430.                                                                                                                                        |
|             |              | INOP ON EXEC                   | Status bit 12, inoperative on execution, is set                                                     | See action code 1430.                                                                                                                                        |
|             |              | INIT STAT ERR                  | Status error occurred in initiator. Bit 1 (busy), bit 6 (program error), bit 3 (inop on selection). | See action code 1430.                                                                                                                                        |
|             |              | WRITE RING IN                  | Status bit 4 did not set or write ring not removed.                                                 | ACST = Actual status                                                                                                                                         |

†All may not be present depending on action code.

TABLE 8-13. LCTTB ACTION CODES (Continued)

| Action Code | Test Section | English Text   | Description                                                                                                                                  | Additional Information                                                        |
|-------------|--------------|----------------|----------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------|
|             |              | WRITE RING OUT | Status bit 4 did not clear or write ring not re-installed.                                                                                   |                                                                               |
|             |              | DID NOT UNLOAD | Rewind/unload did not cause unit to go not ready after tape unloaded.                                                                        |                                                                               |
|             |              | STATUS ERROR   | Status error bit 1 (busy), bit 3 (read after write), bit 6 (program error), bit 8 (short block), bit 11 (short block), or bit 12 (inop/exec) | See action code 1430.                                                         |
| 1438        | 5            | NO PARITY ERR  | Unable to force parity error on seven-track unit                                                                                             | See action code 1430.                                                         |
| 1440        | 1-5          | DATA ERROR     | Data error and good status, based on all data                                                                                                | None                                                                          |
|             |              | DATA ERROR     | Data error and good status, single word error                                                                                                | EXDA = Expected data<br>ACDA = Actual data<br>WORD = Word position in record  |
|             |              | DATA ERROR     | Data error and good status, based on all data                                                                                                | TRK1 to TRK8 = Track number 1 to 8                                            |
|             |              | TRACK FAILURE  | Data error and good status                                                                                                                   |                                                                               |
| 1441        | 8            | POSITION ERROR | Reading wrong record                                                                                                                         | EXDA = Expected data<br>ACDA = Actual data<br>WORD = Word position in record. |
| 1442        | 7            | ERASE FAILURE  | Reading wrong record.                                                                                                                        | See action code 1441.                                                         |
| 1443        | A            | COMPAT ERROR   | Drive compatibility failure                                                                                                                  | See action code 1441.                                                         |
| 1450        | 1-B          | UNEXP INT      | Unexpected interrupt                                                                                                                         | STA1 = Last equipment status<br>ICNT = Ghost interrupt count                  |
| 1451        | 1-B          | NO INTERRUPT   | Timed out waiting for interrupt                                                                                                              | See action code 1430.                                                         |
| 1490        | 1-5          | TRACK 0        | Track 0 data failure                                                                                                                         | FCNT = Failure count                                                          |
| 1491        | 1-5          | TRACK 1        | Track 1 data failure                                                                                                                         |                                                                               |
| 1492        | 1-5          | TRACK 2        | Track 2 data failure                                                                                                                         |                                                                               |

TABLE 8-13. LCTTB ACTION CODES (Continued)

| Action Code | Test Section | English Text | Description                           | Additional Information                                 |
|-------------|--------------|--------------|---------------------------------------|--------------------------------------------------------|
| 1493        | 1-5          | TRACK 3      | Track 3 data failure                  | FCNT = Failure count                                   |
| 1494        | 1-5          | TRACK 4      | Track 4 data failure                  | FCNT = Failure count                                   |
| 1495        | 1-5          | TRACK 5      | Track 5 data failure                  | FCNT = Failure count                                   |
| 1496        | 1-5          | TRACK 6      | Track 6 data failure                  | FCNT = Failure count                                   |
| 1497        | 1-5          | TRACK 7      | Track 7 data failure                  | FCNT = Failure count                                   |
| 1498        | 1-5          | TRACK 8      | Track 8 data failure                  | FCNT = Failure count                                   |
| 14H0        | 1            | FIRST MOTION | Failure on first command to tape unit | STIN = Initialized status<br>STCN = Continuator status |
| 14A2        | 8            | NO FILE MARK | Unable to detect file mark            | See action code 1430.                                  |

# DUAL-CHANNEL COMMUNICATIONS LINE ADAPTER AND OPERATOR'S CONTROL PANEL

Parity type: 1 = Odd  
2 = Even  
3 = None

Frame type: 1 = One-stop bit  
2 = 1.5 stop bits or more

## TEST IDENTIFICATION

15

## TEST NAME

CLA2A

## PURPOSE

The purpose of this test is to detect, isolate, and note all detectable error conditions for the dual-channel communications line adapter and operators control panel.

## PARAMETERS

Initial values for the CLA2A test run parameters are listed in table 8-14.

### Run Parameters A — 15

#### Run Parameters A through 11

Run parameters A through 11 are extended channel descriptions. Their format is as follows:

|                |                |               |   |
|----------------|----------------|---------------|---|
| 11             | 8 7            | 4 3           | 0 |
| Data<br>Length | Parity<br>Type | Frame<br>Type |   |

Data length: 1 = Lower 5 bits  
2 = Lower 6 bits  
3 = Lower 7 bits  
4 = Lower 8 bits

#### Run Parameter 12

Receiver unit number: 1 = Receiver channel 0  
synchronous mode  
3 = Receiver channel 1  
synchronous mode  
5 = Receiver channel 0  
asynchronous mode  
7 = Receiver channel 1  
asynchronous mode

#### Run Parameter 13

Transmitter unit number: 2 = Transmitter channel 0  
synchronous mode  
4 = Transmitter channel 1  
synchronous mode  
6 = Transmitter channel 0  
asynchronous mode  
8 = Transmitter channel 1  
asynchronous mode

#### Run Parameter 14

Data to be transmitted (byte specified): 0A = Byte transmitted

#### Run Parameter 15

Test mode: 0 = Test mode I/O  
1 = Data transmitted from transmitter unit to receiver unit based on unit number and extended channel description using modem or backplane loop back

TABLE 8-14. CLA2A RUN PARAMETER LIST

| Word   | Initial Value (Hex) | Definition                             |
|--------|---------------------|----------------------------------------|
| TESTID | 0015                | Test ID                                |
| PASCNT | 0000                | Pass Count                             |
| ERRCNT | 0000                | Error Count                            |
| 1      | 2080                | Control Word                           |
| 2      | 0001                | Repeat Count                           |
| 3      | 1234                | Section Selection                      |
| 4      | 5678                | Section Selection                      |
| 5      | 9AB0                | Section Selection                      |
| 6      | 0000                | Section Selection                      |
| 7      | 0500                | WES                                    |
| 8      | 00AA                | Micro/Macro Interrupt Line             |
| 9      | 0006                | Logical Unit                           |
| A      | 0411                | R-CH0-Control/Sync/Unit 1              |
| B      | 0411                | T-CH0-Control/Sync/Unit 2              |
| C      | 0411                | R-CH1-Control/Sync/Unit 3              |
| D      | 0411                | T-CH1-Control/Sync/Unit 4              |
| E      | 0411                | R-CH0-Control/Async/Unit 5             |
| F      | 0411                | T-CH0-Control/Async/Unit 6             |
| 10     | 0411                | R-CH1-Control/Async/Unit 7             |
| 11     | 0411                | T-CH1-Control/Async/Unit 8             |
| 12     | 0005                | Unit 5 receives CH0-Async              |
| 13     | 0006                | Unit 6 transmitter CH0-Async           |
| 14     | 000A                | Data                                   |
| 15     | 0000                | 0 - Test Mode<br>1 - With Modems/Cable |

## OVERLAYS

CLA2A uses nine overlays for the overlay version:

| <u>Overlay No.</u> | <u>Test Section No.</u> |
|--------------------|-------------------------|
| 1                  | 0 through 2             |
| 2                  | 3                       |
| 3                  | 4                       |
| 4                  | 5 through 6             |
| 5                  | 7                       |
| 6                  | 8                       |
| 7                  | 9                       |
| 8                  | A                       |
| 9                  | B                       |

## ORGANIZATION

The dual-channel communications line adapter diagnostic consists of eleven test sections.

### Section 1 — Verify Equipment Address/Invalid Commands

The purpose of this section is to ensure that the DCCLA is responding to equipment/station (WES) codes, and that the DCCLA is reporting invalid director codes. Section 1 is composed of two subsections. Subsection 1 verifies that the DCCLA accepts valid WES codes by requesting input channel and active channel status. Subsection 2 verifies that the DCCLA rejects invalid director commands.

Upon completion of section 1, there is a reasonable assurance that a controller is active and the controller is a DCCLA.

## **Section 2 — Verify Common Functions, Test Mode Functions, and External Reject**

The purpose of this section is to ensure that the common function, test mode channel functions, and the external reject circuitry are operative. Section 2 is composed of 12 subsections.

Subsection 1 tests the common function (director code = 4). The subsection ensures that the clear interrupt function only clears the interrupt circuitry and the master reset function clears all circuitry.

Subsection 2 tests the channel clear function (director code = 1) in test mode for channel 0. It ensures that the channel clear function clears the status of the channel to clear state.

Subsection 3 is the same as subsection 2 except that channel 1 is tested.

Subsection 4 reads the status in test mode from channel 0 and compares the status with a test mode constant to ensure that the test mode circuitry is tied high and the remaining statuses are off.

Subsection 5 is the same as subsection 4 except channel 1 is tested.

Subsection 6 tests the request to send function in test mode on channel 0 to ensure that the clear to send status is on.

Subsection 7 is the same as subsection 6 except that channel 1 is tested.

Subsection 8 tests the ADT function in test mode on channel 0 to ensure that the ADT status circuitry is operative.

Subsection 9 is the same as subsection 8 except that channel 1 is tested.

Subsection 10 tests the reject circuitry in test mode on channel 0 for no output/input data function (director code = 0) reject by inputting and outputting without first priming the DCCLA for data transfer.

Subsection 11 is the same as subsection 10 except that channel 1 is tested.

Subsection 12 informs the operator of the status setting of the DCCLA protect status bit with the following message:

CLA2A PROTECT BIT ON (OFF)

## **Section 3 — Verify Data Transfer A/Q, I/O Status Looping of Data, Synchronous Search**

The purpose of this section is to verify the synchronous/asynchronous data loop capability of the DCCLA, the extended channel initialization function, synchronization search, and data byte transfer using status.

Subsection 1 verifies channel 0 synchronous data byte loop capability in test mode by functioning all possible data lengths and parity types in the transmitter/receiver and then looping a data byte from the transmitter to the receiver (four data byte values are looped), using synchronous search and status to control looping.

Subsection 2 is the same as subsection 1 except that the channel 1 is tested.

Subsection 3 verifies channel 0 asynchronous data loop capability in test mode by functioning all possible data lengths, parity types, and framing stop bits in the transmitter/receiver and then looping a data byte from the transmitter to the receiver (four data byte values are looped), using input/output status to control looping.

Subsection 4 is the same as subsection 3 except that channel 1 is tested.

## **Section 4 — Verify Cyclic Redundancy Check Operations**

The purpose of this section is to ensure that the cyclic redundancy check (CRC) generator controller circuitry of the DCCLA is operative by transferring data through the CRC and comparing the generated checkword with a previously computed checkword for equality.

## Section 5 — Verify Basic Operators Panel Operation

The purpose of this section is to set the enable to illuminate the RS232 indicators on the basic operators panel. Visual verification that the proper indicator is enabled is sufficient for the test. All indicators are illuminated with the exception of SQ (signal quality). Each channel is lit for 10 seconds. The following messages are printed out during the test:

LOOK AT BOP 0  
LOOP AT BOP 1

## Section 6 — Utility Section

The purpose of this section is to supply a utility section for the operator to select varying channels, transmitter/receiver pairs, data lengths, parity types, framing stops, and data bytes. If no modification is made to the parameter list, the section is preset to run with channel 0, eight bits of data length, odd parity, one framing stop in asynchronous mode. (See parameter sections A through 15.)

## Section 7 — Negative Testing of Parity and Lost Data Verification

The purpose of this section is to ensure that the parity circuitry and lost data circuitry are operative. Section 7 is composed of two subsections.

Subsection 1 loops a data byte from a transmitter primed for 8-bit even parity to a receiver primed for 8-bit odd parity. If an error is not detected, a primary error message is output.

Subsection 2 loops three data bytes to a receiver expecting lost data circuitry to detect lost data. If an error is not detected, a primary error message is output.

## Section 8 — Single-Channel ADT Transfer

The purpose of this section is to verify that each channel of the DCCLA operation is asynchronous to ADT.

Subsection 1 verifies channel 0 asynchronous multiple data loop capability in test mode by functioning all possible data lengths and parity types in the transmitter/receiver, and then looping multiple data bytes from the transmitter to the receiver (four data byte types are looped) using ADT to loop the data bytes.

Subsection 2 is the same as subsection 1 except that channel 1 is tested.

## Section 9 — Negative Testing

The purpose of this section is to perform negative testing of the DCCLA board; however, negative testing is incomplete at the end of this section and is completed in section B.

Subsection 1 verifies that a fill character can be looped and is equal for transmission channels 0 and 1 and for receiver channels 0 and 1. The setting and clearing of the data not available status is also verified here.

Subsection 2 verifies that the frame status bit is operative by looping a 7-bit character to a 6-bit receiver expecting frame error.

Subsection 3 verifies an async break by requesting a break function during data transmission. A framing error is expected.

## Section A — Timing Rates

The purpose of this section is to perform timing analysis on the DCCLA board and report the results.

Subsection 1 verifies that channels 0 and 1 loop in synchronous mode at a test mode clock speed of 9600 baud/BPS.

Subsection 2 informs the operator of the asynchronous test mode clock baud rate.

## Section B — Negative Testing

The purpose of this section is to complete negative testing of the DCCLA board not processed by section 9.

Subsection 1 verifies the error interrupt capability of channels 0 and 1 by looping an incorrectly functioned (to ensure error) data buffer from transmission channel 0 to receiver channel 0.

## MESSAGES

### Action Codes

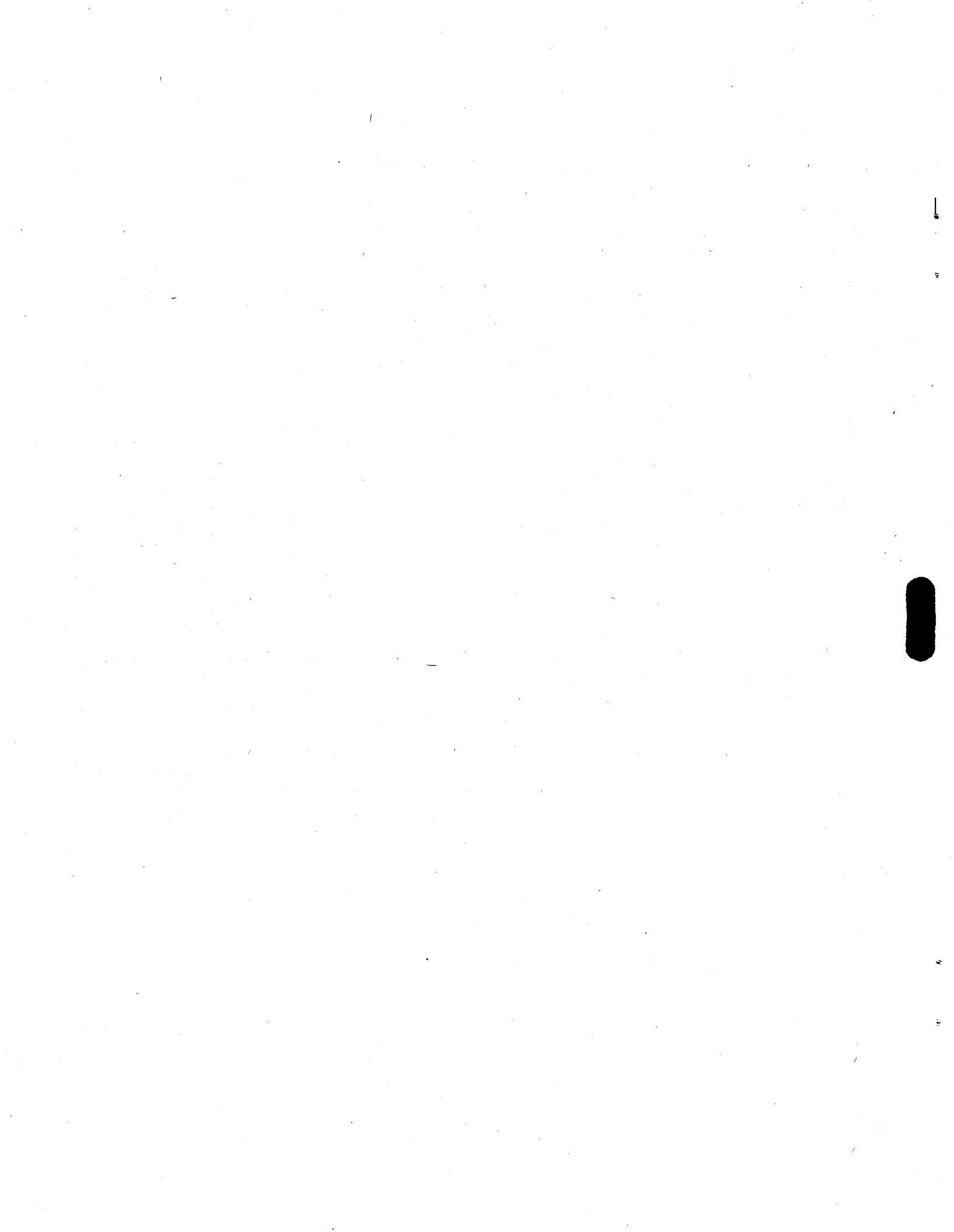
Table 8-15 lists the CLA2A action codes.

TABLE 8-15. CLA2A OUTPUT MESSAGES

| Action Code | Test Section | English Text    | Description                                                                 | Additional Information                                                |
|-------------|--------------|-----------------|-----------------------------------------------------------------------------|-----------------------------------------------------------------------|
| 1511        | 1            | NO I/O RESPONSE | Internal reject                                                             | None                                                                  |
| 1512        | 1            | NO I/O RESPONSE | External reject                                                             | None                                                                  |
| 1513        | 1            | NO I/O RESPONSE | Illegal director code accepted                                              | None                                                                  |
| 1515        | 2            | FUNCTION/STATUS | Test mode status not up after test mode function                            | None                                                                  |
| 1516        | 2            | FUNCTION/STATUS | Test mode status cleared by a channel clear                                 | None                                                                  |
| 1517        | 2            | FUNCTION/STATUS | Test mode status not cleared by a channel clear                             | None                                                                  |
| 1518        | 2            | FUNCTION/STATUS | Channel not cleared to ready after channel clear                            | None                                                                  |
| 1519        | 2            | FUNCTION/STATUS | Request to SEND/CLEAR to send status not up after test mode request to send | None                                                                  |
| 151A        | 2            | FUNCTION/STATUS | ADT IN/OUT status not up after test mode ADT IN/OUT function request        | None                                                                  |
| 151B        | 2            | FUNCTION/STATUS | Reject on input/output                                                      | None                                                                  |
| 153F        | 3-B          | SECONDARY INFO  | Master clear error                                                          | ERRC = Error code                                                     |
| 1590        | 3-B          | SECONDARY INFO  | Negative test parity failure                                                | 01 = Test detected internal reject.                                   |
| 1591        | 3-B          | SECONDARY INFO  | Negative test lost data failure                                             | 02 = Test detected external reject.                                   |
| 1593        | 9-B          | SECONDARY INFO  | No error interrupt                                                          | 40 = Framing error detected                                           |
| 1594        | 9-B          | SECONDARY INFO  | No fill character transmitted                                               | 41 = Lost data error detected                                         |
|             |              |                 |                                                                             | 42 = Software detected parity error bit but none selected in hardware |
|             |              |                 |                                                                             | 43 = Parity error                                                     |
|             |              |                 |                                                                             | 44 = Hardware detected parity but failed to generate parity bit       |

TABLE 8-15. CLA2A OUTPUT MESSAGES (Continued)

| Action Code | Test Section | English Text   | Description                           | Additional Information                                                          |
|-------------|--------------|----------------|---------------------------------------|---------------------------------------------------------------------------------|
| 1595        | 9-B          | SECONDARY INFO | No data not available status          | 45 = Compare error of data                                                      |
| 1596        | 9-B          | SECONDARY INFO | No data not available                 | 46 = Software detected parity/hardware failed to detect parity.                 |
| 1597        | 9-B          | SECONDARY INFO | No frame error status                 | 51 = Kernel detected internal reject for ADT.                                   |
| 1598        | 9-B          | SECONDARY INFO | No asynchronous break detected        | 52 = Kernel detected external reject for ADT.                                   |
| 15EE        | 9-B          | SECONDARY INFO | Driver detected error                 | 53 = Time-out-error interrupt failure on ADT                                    |
|             |              |                |                                       | 54 = Interrupt on not ADT-EOP or error                                          |
|             |              |                |                                       | 55 = Status failure on functioning channel for ADT                              |
|             |              |                |                                       | 56 = Error interrupt on ADT read                                                |
|             |              |                |                                       | 7A = Status failure for priming channel for data input/output                   |
|             |              |                |                                       | 7B = Status failure for inputting data                                          |
|             |              |                |                                       | 7D = Status failure for outputting data                                         |
|             |              |                |                                       | 7E = Sync search failure                                                        |
|             |              |                |                                       | STAT = Last status of the DCCLA board                                           |
|             |              |                |                                       | DATI = Data transmitted                                                         |
|             |              |                |                                       | PDTA = Physical device table address                                            |
|             |              |                |                                       | ECCC = Extended channel control                                                 |
|             |              |                |                                       | LOGU = Logical unit                                                             |
|             |              |                |                                       | WESC = Equipment station channel used                                           |
|             |              |                |                                       | TPLA = Test parameter list address                                              |
|             |              |                |                                       | DAT2 = Data input                                                               |
|             |              |                |                                       | DAT3 = Length of data/buffer address (if used in request)                       |
| 15FF        | All          | LLA BOARD BAD  | Issued for all primary error messages | ERRC } Issued only if master clear of<br>STAT } board is attempted and rejected |



These tests are provided to allow maximum multiplexing in a minimum core configuration (16K). Each of these tests consists of selected sections from the standard device tests. The descriptions for each test and section are identical to the standard device test descriptions. Other multiplexing combinations are allowed depending on memory size. Table 9-1 lists the

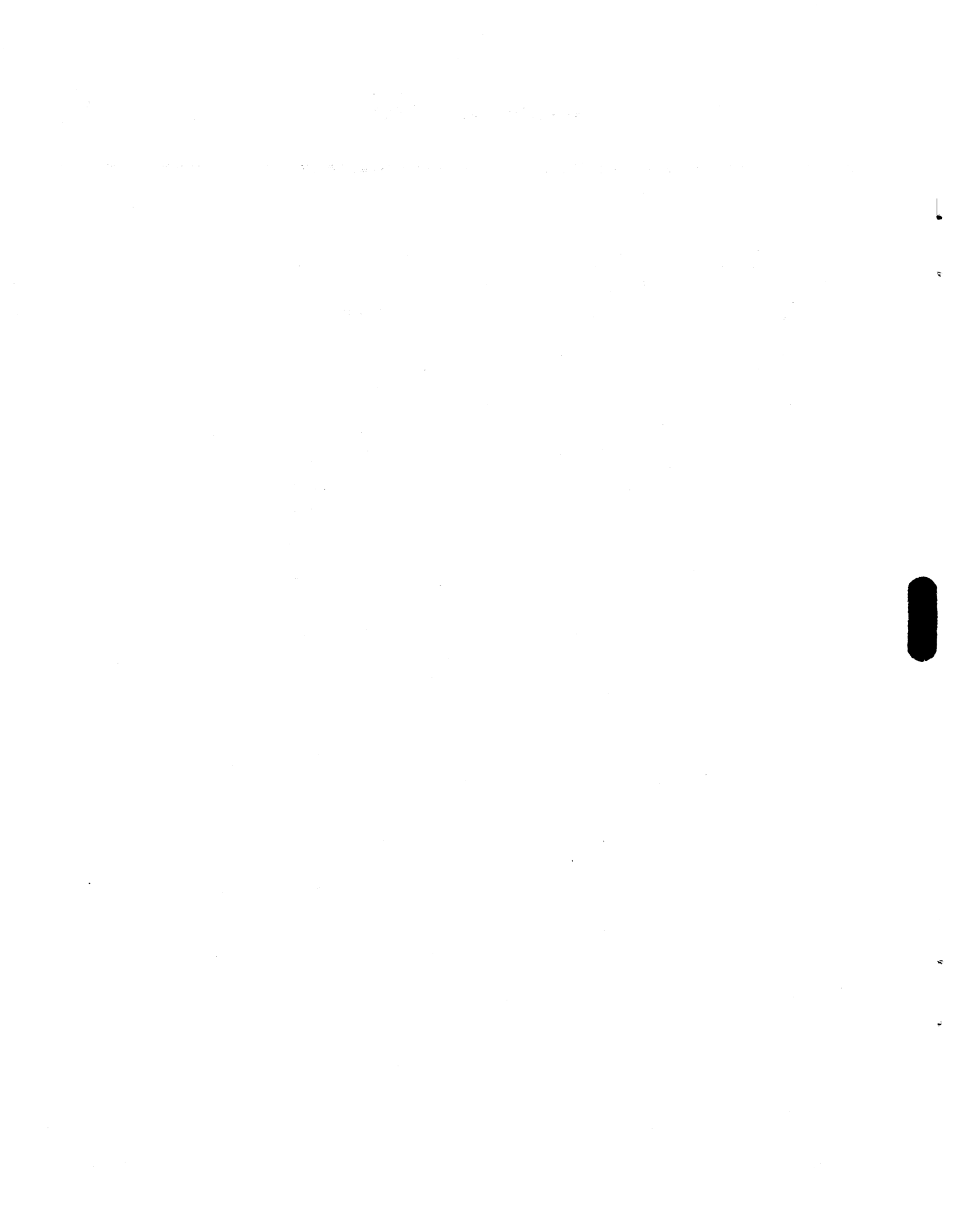
multiplex tests and their names, test IDs, and the non-overlay tests and test sections used.

### RESTRICTIONS

Tests apply only in a non-overlay version.

TABLE 9-1. MULTIPLEXING TESTS

| Multiplex Test | Test ID (Hexadecimal) | Non-Overlay Test and Sections Used |
|----------------|-----------------------|------------------------------------|
| C104M          | 18                    | CRUT1 0, 2                         |
| LCTTM          | 19                    | LCTTB 0, 9, A, 10                  |
| L408M          | 1A                    | LP408 0, 2                         |
| CLA2M          | 1B                    | CLA2A 0, 8                         |



# GLOSSARY

A

|                         |                                                                                                                                                                                                                                                                                                                                                                         |                         |                                                                                                                                                                                                                                                                                                     |
|-------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| A/Q Transfer            | An input/output channel transfer through the A register                                                                                                                                                                                                                                                                                                                 | Burst Input             | Transmission of records with an interval of time between transmissions                                                                                                                                                                                                                              |
| Absolute Address        | <ol style="list-style-type: none"> <li>1. An address that is permanently assigned by the machine designer to a storage location</li> <li>2. A pattern of characters that identifies a unique storage location without further modification</li> <li>3. Synonymous with machine address, specific address</li> </ol>                                                     | CDT                     | Conversational display terminal                                                                                                                                                                                                                                                                     |
| Absolute Binary Program | A program that must be loaded according to specific logical addresses                                                                                                                                                                                                                                                                                                   | Checksum                | A summation of digits or bits used for checking                                                                                                                                                                                                                                                     |
| Action Code             | A hexadecimal four-digit number that leads the operator to an entry in the diagnostic decision logic table (DDLT) in the hardware maintenance manual. The leftmost two digits are the test ID that detected the error and the rightmost two digits are the error code. Each action code is unique to a specific test and test error condition.                          | DDLT                    | Diagnostic decision logic table                                                                                                                                                                                                                                                                     |
| Action Message          | Same as English text message. An action message instructs the operator to take some action.                                                                                                                                                                                                                                                                             | Deadstart               | Hardware controlled loading of the main memory, registers, and function control register as well as the initiation of that loaded program                                                                                                                                                           |
| ADT Mode                | Auto data transfer mode. Pseudo direct-memory transfer of data blocks to or from any device.                                                                                                                                                                                                                                                                            | Diagnostic Error        | An error detected by ODS diagnostic test containing pertinent information regarding the test, equipment, and exact cause of error                                                                                                                                                                   |
| ASCII                   | American National Standard Code for Information Interchange; the standard code, using a coded character set consisting of 7-bit coded characters (8 bits including parity check), used for information interchange among data processing systems, communication systems, and associated equipment. The ASCII set consists of control characters and graphic characters. | Emulation               | The process combining hardware and firmware design in which one processor (emulator) executes programs designed for a different processor, even though one-to-one hardware correspondence does not exist                                                                                            |
| Basic Instruction       | Basic 1700 computer instruction repertoire. Also referred to as type 1 instructions.                                                                                                                                                                                                                                                                                    | English Text Message    | Sixteen-character description accompanying an action code                                                                                                                                                                                                                                           |
| BOP                     | Basic operators panel                                                                                                                                                                                                                                                                                                                                                   | Enhanced Instruction    | Instructions used to enhance the 1700 basic instructions. Also referred to as type 2 instructions                                                                                                                                                                                                   |
|                         |                                                                                                                                                                                                                                                                                                                                                                         | EOD                     | End-of-deck card                                                                                                                                                                                                                                                                                    |
|                         |                                                                                                                                                                                                                                                                                                                                                                         | EOF                     | End-of-file card                                                                                                                                                                                                                                                                                    |
|                         |                                                                                                                                                                                                                                                                                                                                                                         | Error Code              | Rightmost two digits of action code                                                                                                                                                                                                                                                                 |
|                         |                                                                                                                                                                                                                                                                                                                                                                         | Executive Error Message | An error caused by the monitor or executive                                                                                                                                                                                                                                                         |
|                         |                                                                                                                                                                                                                                                                                                                                                                         | Fatal Error             | An error that causes the system to come to an immediate halt                                                                                                                                                                                                                                        |
|                         |                                                                                                                                                                                                                                                                                                                                                                         | FCR                     | Function control register                                                                                                                                                                                                                                                                           |
|                         |                                                                                                                                                                                                                                                                                                                                                                         | Flag                    | <ol style="list-style-type: none"> <li>1. A character or bit that signals the occurrence of some condition, such as the end of a word</li> <li>2. An indicator (program or hardware initiated) used frequently to tell some later part of a program that some condition occurred earlier</li> </ol> |

|                           |                                                                                                                                                                                                                                                                                                                                     |                          |                                                                                                                 |
|---------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------|-----------------------------------------------------------------------------------------------------------------|
| Ghost Interrupt           | An unexpected interrupt from a peripheral device or an unused line                                                                                                                                                                                                                                                                  |                          | as another element that executed previously.                                                                    |
| Informative Message       | A message where no action is required                                                                                                                                                                                                                                                                                               | PE                       | Parity error                                                                                                    |
| Kernel Driver             | A program that processes another program's request to operate an I/O device. It contains only the essentials needed to operate an I/O device, usually without any formatting, data conversion or error recovery. Error detection is considered a fundamental requirement.                                                           | PF                       | Protect fault                                                                                                   |
| LCTT                      | Low cost tape transport                                                                                                                                                                                                                                                                                                             | Primary Error            | Any error causing the machine to halt for other than normal program stops or informative messages               |
| Load Path                 | All the hardware components required to load a binary object program, instructions, memory, and the load device                                                                                                                                                                                                                     | Privileged Instruction   | An instruction that cannot be executed by an unprotected program                                                |
| Logical Unit              | A number that can be equated to any one of a variety of peripheral units for use by software.                                                                                                                                                                                                                                       | Protected Instruction    | Instruction with protect bit set                                                                                |
| LSB                       | Least significant bit                                                                                                                                                                                                                                                                                                               | PW                       | Power failure                                                                                                   |
| Macro Go                  | I@ entered from the CDT keyboard                                                                                                                                                                                                                                                                                                    | RBD                      | Relocatable binary deck                                                                                         |
| Macro Halt                | A selective stop switch is set in the FCR. A selective stop command is executed or an H: is entered.                                                                                                                                                                                                                                | RTC                      | Real-time clock. A device that will interrupt the processor at a given time (for example, once every 3.3 msec.) |
| Manual Interrupt          | CNTRL/BELL key and SHIFT key pressed simultaneously                                                                                                                                                                                                                                                                                 | Secondary Error          | Any non-fatal error, such as informative messages or designated program stops                                   |
| Monitor                   | The supervisory routine in an operating system that coordinates and controls the operation of user and system programs                                                                                                                                                                                                              | Section                  | A selectable portion of a diagnostic test series                                                                |
| MSB                       | Most significant bit                                                                                                                                                                                                                                                                                                                | Section Selection Word   | Words 3 through 6 of the run parameter list                                                                     |
| Multi-level Indirect Test | A test to determine direct or indirect addressing (based on examination of bit 15 of a test address)                                                                                                                                                                                                                                | Skip Switch              | A bit that can be set in the FCR to determine instructions to be skipped. Used for program control              |
| ODS                       | Operational Diagnostic System                                                                                                                                                                                                                                                                                                       | Slewing                  | Passing data until a desired pattern is sensed                                                                  |
| OV                        | Overflow of volatile storage                                                                                                                                                                                                                                                                                                        | Software Induced Failure | A failure caused by a software program                                                                          |
| Overlay                   | A technique that is used for processing a program whose total storage requirements for instructions exceed available memory. The program is divided into elements that are brought into memory at different points of processing. An element of an overlay program, when brought into memory, may occupy the same storage locations | Solid Failure            | A failure that occurs in the same way at the same place every time                                              |
|                           |                                                                                                                                                                                                                                                                                                                                     | Stack Memory             | Refers to an 8K segment of macro memory (core stack).                                                           |
|                           |                                                                                                                                                                                                                                                                                                                                     | Stand-Alone Program      | A program that does not run under control of a monitor or with other programs                                   |
|                           |                                                                                                                                                                                                                                                                                                                                     | Subsection               | A repeatable portion of a section                                                                               |
|                           |                                                                                                                                                                                                                                                                                                                                     | Suspension Message       | A message issued whenever a diagnostic test is suspended from execution                                         |
|                           |                                                                                                                                                                                                                                                                                                                                     | Transient Failure        | A failure that does not occur consistently                                                                      |

Volatile Core

Memory reserved for intermediate storage of data

Worst Case

That which creates maximum stress or consumes maximum time



# ROUTINES AVAILABLE TO ODS DIAGNOSTICS

B

Tables B-1 through B-4 list all of the routines that are available for usage by the ODS diagnostics. Most are callable from a FORTRAN program unless stated otherwise. These routines are grouped into four categories. The first category includes all routines that are available as monitor routines in levels I and II; the second category includes those routines that are available as monitor routines only in level I; the third is the routines

that are available as monitor routines for level II; the fourth category includes those programs that are only available if they are absolutized with the test in either levels I or II. Any routine that falls into the second category also falls into category four for a level II test. For a more detailed explanation and the code for each of the routines, check the program listing.

TABLE B-1. LEVEL I AND LEVEL II MONITOR ROUTINES

| Name   | Function                                                                                                                                                                                                                                         |
|--------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| ENDSEC | Informs the ODS monitor when a diagnostic section is done                                                                                                                                                                                        |
| ERROR  | Called by the diagnostic sections to display error action messages and data                                                                                                                                                                      |
| GETPAR | Picks up one word from a parameter list                                                                                                                                                                                                          |
| OUTMSG | Provides the means for a diagnostic section to display information to the operator on the CDT                                                                                                                                                    |
| PUTPAR | Used to put a word into the test's parameter list                                                                                                                                                                                                |
| Q8PKUP | Examines the next parameter address in a list of parameters passed to a subroutine or function. If the parameter address is FORTRAN relative, the parameter's address is absolutized. Q8PKUP will return the absolute address in the A register. |
| Q8PREP | Used to determine the absolute address of the subroutine or function that calls Q8PREP. This enables subroutine Q8PKUP to absolutize any FORTRAN relative parameters passed to the routine.                                                      |
| RSUBSC | Used to determine if repeat subsection, stop at end of subsection, or stop at end of subsection if error has been selected by the operator. Returns to the program with A=1 if repeat has been selected, or else A=0.                            |
| SUSPND | Subroutine will suspend the execution of a diagnostic section when called. Control is returned to the program when a GO command has been entered for the test.                                                                                   |

TABLE B-2. LEVEL I ONLY MONITOR ROUTINES

| Name   | Function                                                               |
|--------|------------------------------------------------------------------------|
| ASCHEX | Converts an ASCII buffer to a hexadecimal value (not FORTRAN callable) |
| HEXASC | Converts a hexadecimal value to an ASCII buffer (not FORTRAN callable) |

TABLE B-3. LEVEL II ONLY MONITOR ROUTINES

| Name   | Function                                                                                                                                                                                                                                                                                                                                       |
|--------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| ABRRST | Called by diagnostic sections to detect operator request to either abort or restart a test (level II only)                                                                                                                                                                                                                                     |
| BIGBEN | Used to get the current value of the system clock (level II only)                                                                                                                                                                                                                                                                              |
| CHGLIN | Used in initialization sections to set up the interrupt lines and equipment number (level II only)                                                                                                                                                                                                                                             |
| LINK   | Returns the address of the test's parameter list which is passed in Q as the beginning of the test. A call to LINK must be the first thing done in all test sections.                                                                                                                                                                          |
| PDTADR | Gets the absolute address of a physical device table for a device to be tested                                                                                                                                                                                                                                                                 |
| Q8STP  | Satisfies the FORTRAN compiler, which will append a call Q8STP at the end of every program. The diagnostic test should call ENDSEC as the end of the section and this does not return to the program. If Q8STP is ever entered there is a fatal error condition and the processor will be hung by executing an 18FF <sub>16</sub> instruction. |

TABLE B-4. ROUTINES ABSOLUTIZED IN LEVEL I OR LEVEL II

| Name   | Function                                                                               |
|--------|----------------------------------------------------------------------------------------|
| ACTUAL | Returns with the absolute external address or value of parameter passed to it          |
| ASCHX  | Converts an ASCII buffer to a hexadecimal value (FORTRAN compatible)                   |
| GETCAR | Fetches a character from specified buffer and returns its value to the calling program |
| HXASC  | Same as HEXASC except that it is callable by a FORTRAN program                         |
| PUTCAR | Places one character into a buffer as specified by the calling program                 |

# DEADSTART FORMAT

C

The ODS LODCHK test is provided in a format known as deadstart format. The data generated for this format is in ASCII codes, which are read into and acted upon by either the panel interface hardware or the panel simulation firmware (if the panel hardware has been removed) during deadstart.

As long as the processor is in deadstart mode, the card reader interface will cause cards to be fed and the data on those cards transmitted serially to the panel interface hardware/firmware. Deadstart mode is initiated by pushing the deadstart button on the processor or the AUTOLOAD button on the BOP. Deadstart mode is terminated by the data on the deadstart cards.

The LODCHK deadstart deck is made up of three parts. The first part is the initialization data which sets up the function control register (FCR) for the rest of the deadstart operation and sets the P register to the address at which to start loading the program data. (See figure C-1.)

The second part of the LODCHK deadstart deck is the memory data cards. Each of the words of the LODCHK program is loaded by having four hexadecimal characters followed by a G on the card. A maximum of eight words can be contained on a single data card. An example of this card is given in figure C-2.

The third part of the LODCHK deadstart deck terminates the loading of the LODCHK program. After all of the data cards have been read, the following steps are performed:

1. The P register is set to the address of the first instruction to be executed in LODCHK.
2. The FCR register is set up to the value for the execution of LODCHK.
3. The program (LODCHK) is started.

An example of the card used to perform these steps is given in figure C-3.

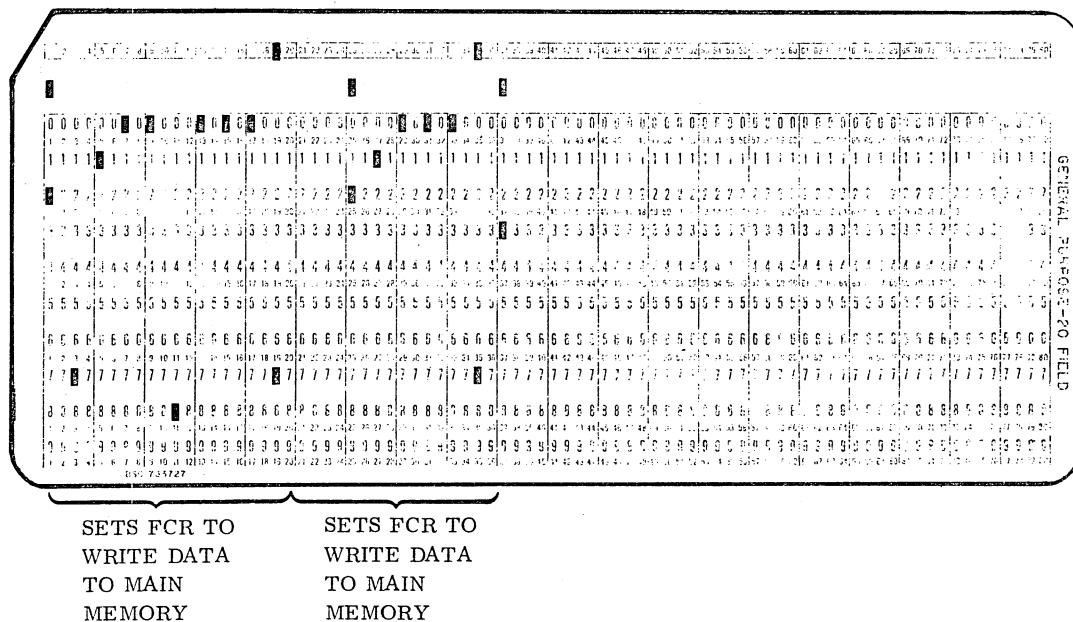


Figure C-1. First Part of LODCHK Deadstart Deck

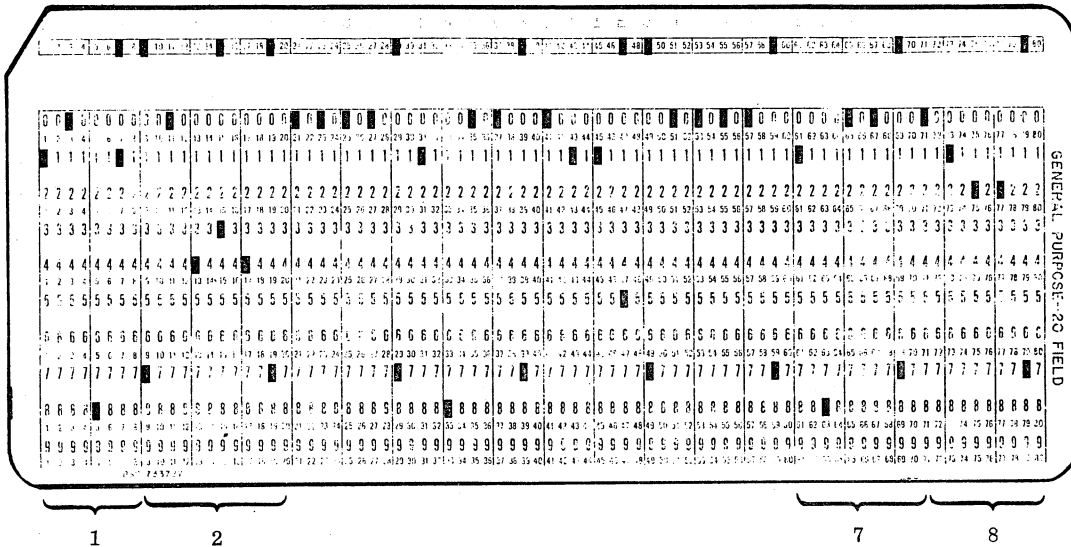


Figure C-2. Second Part of LODCHK Deadstart Deck

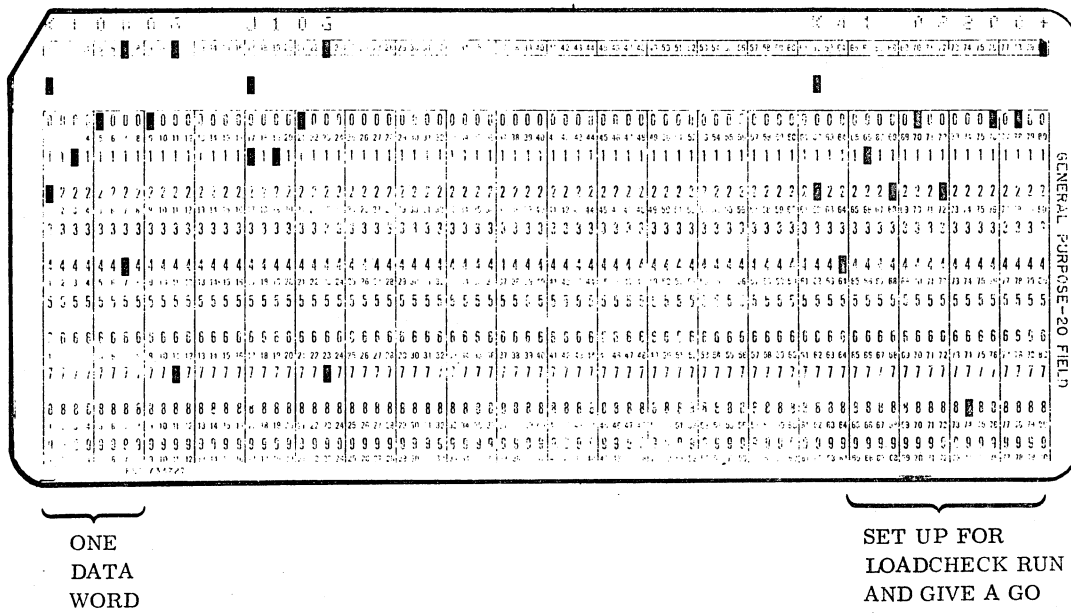


Figure C-3. Third Part of LODCHK Deadstart Deck

# TWELVE-BIT ABSOLUTE BINARY CARD FORMAT

D

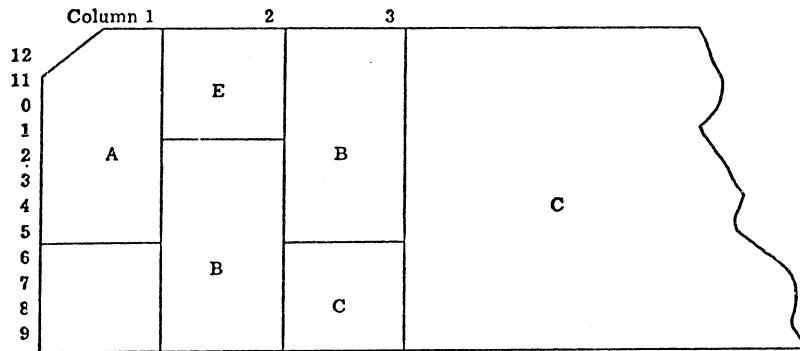
All tests and monitors provided for the ODS system are in the 12-bit absolute binary card format.

All of the absolute cards have seven- and nine-punched rows with the sequence number in rows 0 through 5, 11

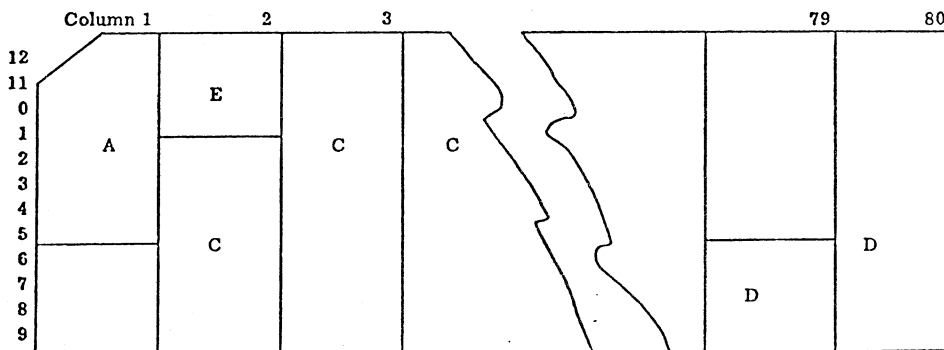
and 12. The checksum at the end of the cards is such that the total of all data punched on the card is zero.

A pictorial description of the 12-bit absolute card format is given in figure D-1.

## First Card

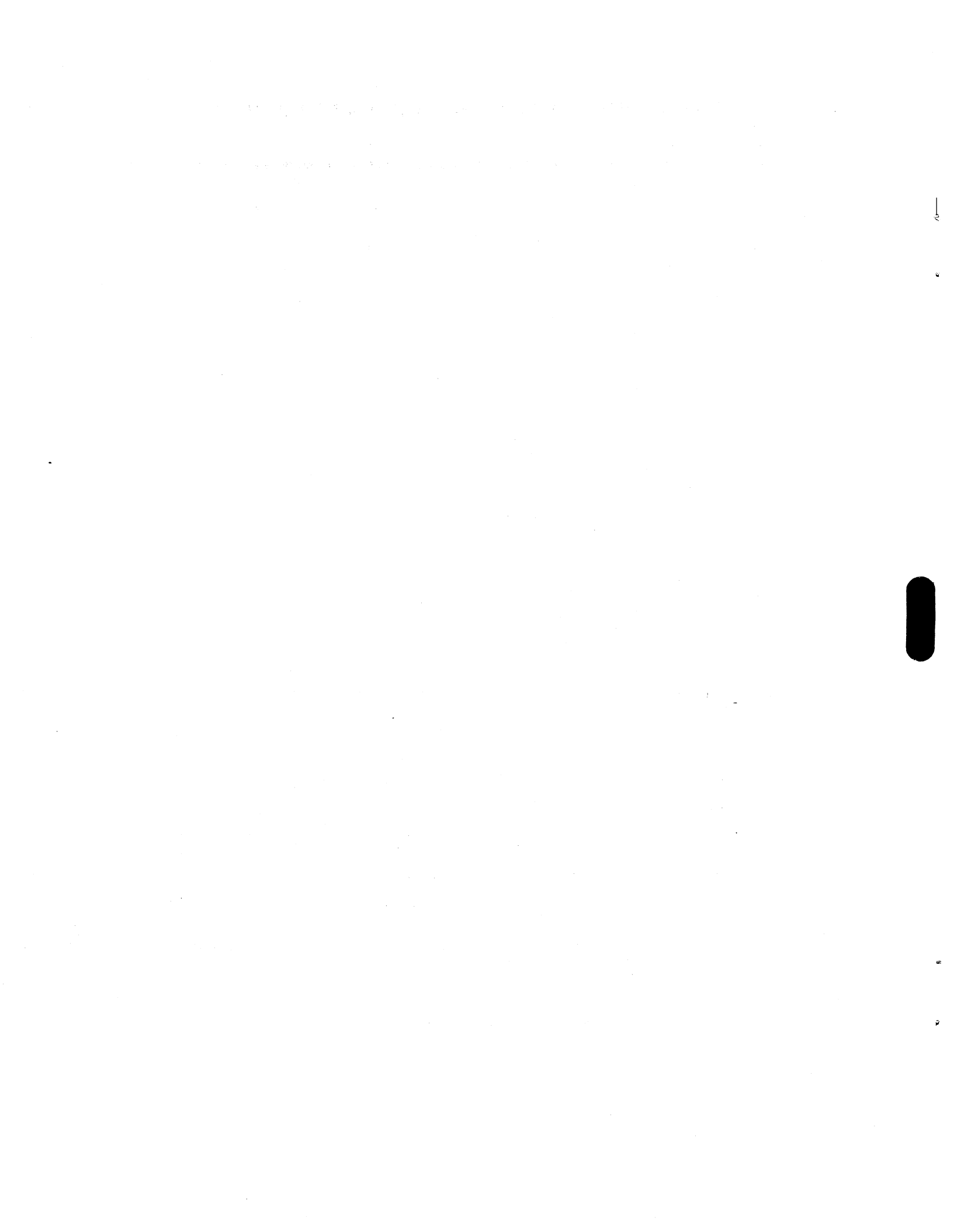


## Subsequent Cards



- Where:
- A is the sequence number (column 1, rows 12 through 5).
  - B is the complemented record length (column 2, rows 2 through 9; column 3, rows 12 through 5 on the first card).
  - C is the data (first card starts in column 3, row 6; other cards start in column 2, row 2).
  - D is a 16-bit checksum (follows the last data word of a record).
  - E is reserved (column 2, rows 12 through 1).

Figure D-1. 12-Bit Absolute Card Format



# LEVEL I RECORD ORGANIZATION

E

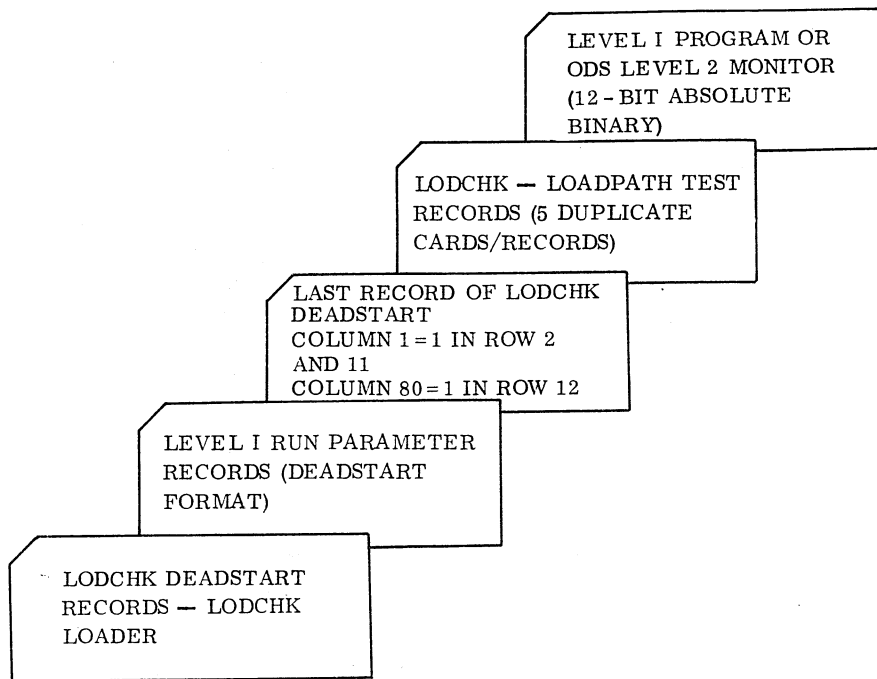


Figure E-1. Level I Records

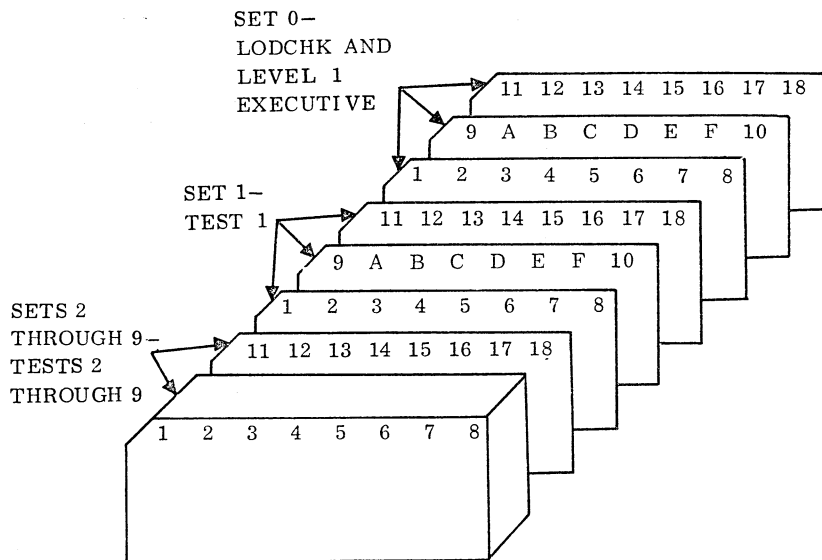


Figure E-2. Level 1 Run Parameter Records

TABLE E-1. LODCHK AND LEVEL I PARAMETERS

| Test No.    | Parameter No. | Preset Value | Description                                                        |
|-------------|---------------|--------------|--------------------------------------------------------------------|
| LODCHK      | 1             | 4 3 5 2      | Identification code (IDC) — CR (card reader)                       |
|             | 2             | 0 0 0 B      | Equipment code — Card reader                                       |
|             | 3 through 16  | 0 0 0 0      | Reserve                                                            |
|             | 17            | 0 0 0 0      | Master control word (for level I)                                  |
|             | 18            | 0 0 0 0      | FWA of the loader (placed by the loader)                           |
| 1 through 9 | 1             | —            | Test ID                                                            |
|             | 2             | —            | Pass count                                                         |
|             | 3             | —            | Error count                                                        |
|             | 4             | —            | Control word                                                       |
|             | 5             | —            | Repeat count                                                       |
|             | 6 through 9   | —            | Section selection, four bits per section, 16 sections (four words) |
|             | 10            | —            | Equipment address                                                  |
|             | 11            | —            | Interrupt lines                                                    |
|             | 12            | —            | Logical unit                                                       |
|             | 13 through 24 | —            | Test-defined parameter list (12 words)                             |

Figure E-3 is an example of the three parameter cards (eight parameters per card) for LODCHK. The space between each character is to allow time for the panel

interface to react to the character. The G is the termination to the DEADSTART for each parameter.

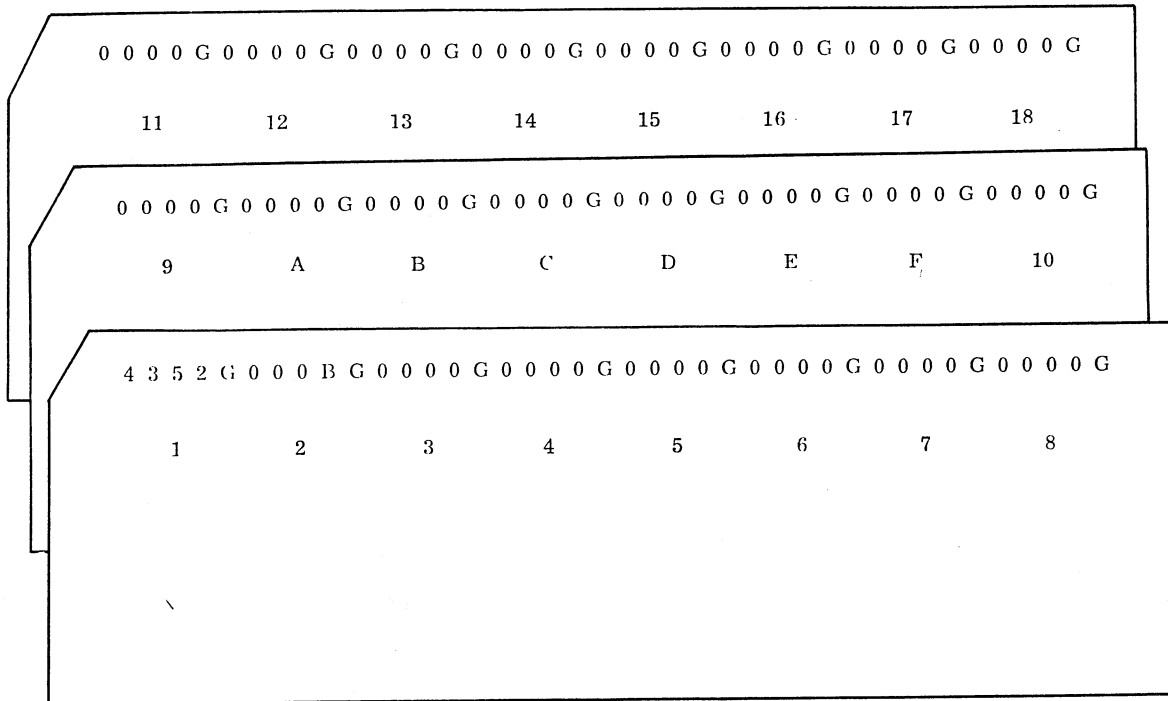


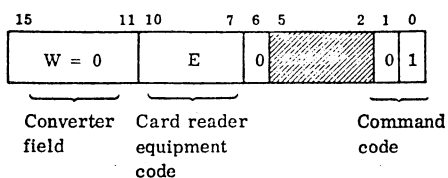
Figure E-3. LODCHK Parameter Cards



CARD READER CONTROLLER

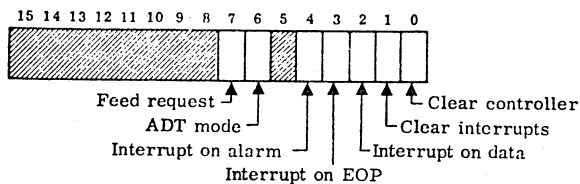
FUNCTION

Q Register



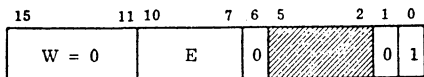
| Command Code |    | Read              | Write             |
|--------------|----|-------------------|-------------------|
| Q1           | Q0 |                   |                   |
| 0            | 0  | Data Transfer     | Illegal           |
| 0            | 1  | Director Status 1 | Director Function |
| 1            | 0  | Illegal           | Test Mode         |
| 1            | 1  | Director Status 2 | Illegal           |

A Register

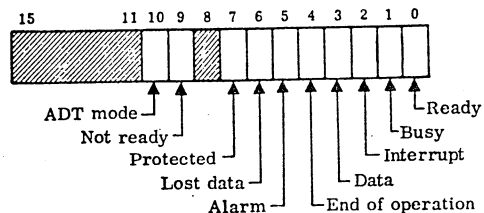


DIRECTOR STATUS 1

Q Register

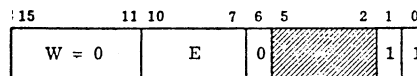


A Register

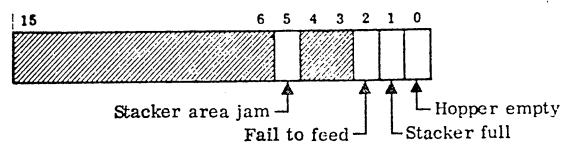


DIRECTOR STATUS 2

Q Register

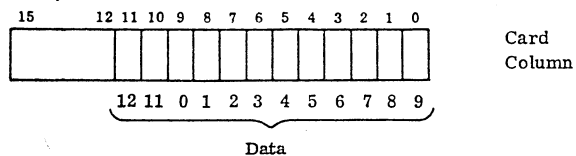


A Register



DATA TRANSFER

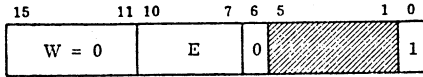
A Register



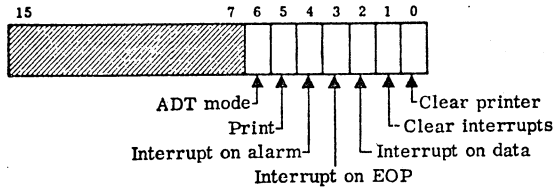
# LINE PRINTER/CONTROLLER

## FUNCTION

### Q Register

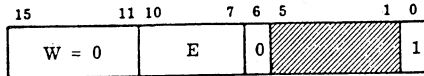


### A Register

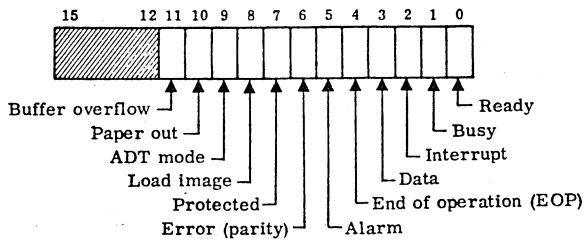


## DIRECTOR STATUS

### Q Register

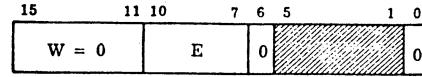


### A Register



## DATA TRANSFER

### Q Register



### A Register

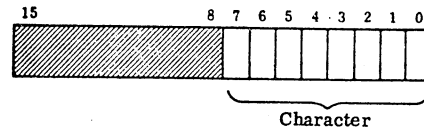


TABLE 4. CHARACTER BITS IN A REGISTER

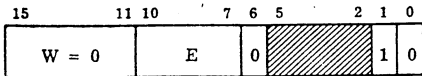
| 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 | Function                             |
|----|----|----|----|----|----|----|----|--------------------------------------|
|    |    |    |    |    |    |    |    | <b>Horizontal Control</b>            |
| X  | 0  | X  | X  | X  | X  | 0  | 0  | Suppress space                       |
| X  | 0  | X  | X  | X  | X  | 0  | 1  | Single space                         |
| X  | 0  | X  | X  | X  | X  | 1  | 0  | Double space                         |
| X  | 0  | X  | X  | X  | X  | 1  | 1  | Triple space                         |
|    |    |    |    |    |    |    |    | <b>Vertical Control</b>              |
| X  | 1  | X  | X  | 0  | 0  | 0  | 0  | Channel 1 top of file (TOF)          |
| X  | 1  | X  | X  | 0  | 0  | 0  | 1  | Channel 2 bottom of file (BOF)       |
| X  | 1  | X  | X  | 0  | 0  | 1  | 0  | Channel 3                            |
|    |    |    |    |    |    |    |    | ⋮                                    |
| X  | 1  | X  | X  | 1  | 0  | 1  | 1  | Channel 12                           |
| X  | 1  | X  | X  | 1  | 1  | 0  | 0  | } Illegal as vertical format control |
| X  | 1  | X  | X  | 1  | 1  | 0  | 1  |                                      |
| X  | 1  | X  | X  | 1  | 1  | 1  | 0  |                                      |
| X  | 1  | X  | X  | 1  | 1  | 1  | 1  |                                      |

Notes: 1. X implies not significant.  
 2. When illegal vertical format control character is issued, it is decoded as if bit 5 = 0.  
 3. First character output is used as control character.

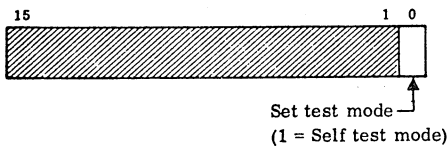
# CARD READER AND LINE PRINTER CONTROLLER TEST MODE

## FUNCTION

### Q Register



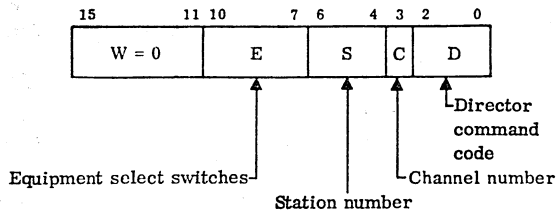
### A Register



# DUAL-LINE COMMUNICATIONS LINE ADAPTER (DCCLA)

## FUNCTION

### Q Register

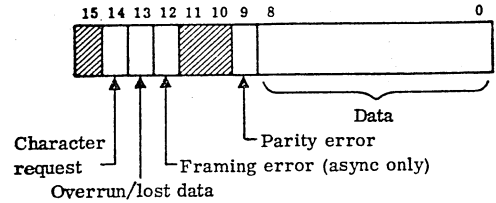


## DIRECTOR CODES

| 2 | 1 | 0 | Read           | Write               |
|---|---|---|----------------|---------------------|
| 0 | 0 | 0 | Data transfer  | Data transfer       |
| 0 | 0 | 1 | Channel status | Channel function    |
| 0 | 1 | 0 | Active channel | Not used            |
| 0 | 1 | 1 | Not used       | Not used            |
| 1 | 0 | 0 | Not used       | Common function     |
| 1 | 0 | 1 | Not used       | Initialize function |
| 1 | 1 | 0 | Input CRC      | CRC data            |
| 1 | 1 | 1 | Not used       | Output CRC OPR      |

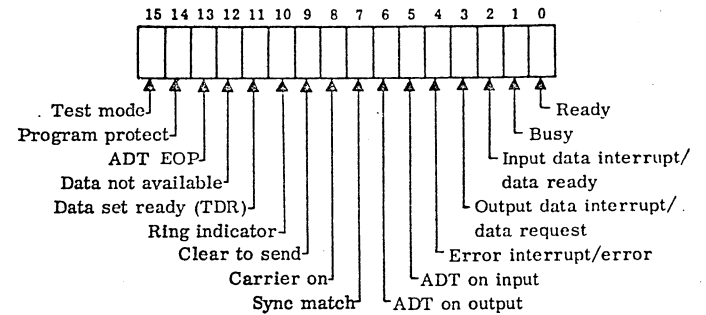
# INPUT DATA TRANSFER

## A Register



# EXTENDED CHANNEL CONTROL TRANSMITTER

## A Register



## Transmitter Control Word Format for Synchronous Operation

| Control Word Format† |   |   |   |   |   | Character Format |   |           |                  |
|----------------------|---|---|---|---|---|------------------|---|-----------|------------------|
| W                    | W | M | M | C | C | P                | P | Data Bits | Added Parity Bit |
| 2                    | 1 | 2 | 1 | 2 | 1 | 2                | 1 |           |                  |
| 7                    | 6 | 5 | 4 | 3 | 2 | 1                | 0 |           |                  |
| 0                    | 0 | 1 | 0 | 0 | 0 | 0                | 0 | 5         | Odd              |
| 0                    | 0 | 1 | 0 | 0 | 0 | 0                | 1 | 5         | Even             |
| 0                    | 0 | 1 | 0 | 0 | 0 | 1                | 0 | 5         | None             |
| 0                    | 1 | 1 | 0 | 0 | 0 | 0                | 0 | 6         | Odd              |
| 0                    | 1 | 1 | 0 | 0 | 0 | 0                | 1 | 6         | Even             |
| 0                    | 1 | 1 | 0 | 0 | 0 | 1                | 0 | 6         | None             |
| 1                    | 0 | 1 | 0 | 0 | 0 | 0                | 0 | 7         | Odd              |
| 1                    | 0 | 1 | 0 | 0 | 0 | 0                | 1 | 7         | Even             |
| 1                    | 0 | 1 | 0 | 0 | 0 | 1                | 0 | 7         | None             |
| 1                    | 1 | 1 | 0 | 0 | 0 | 0                | 0 | 8         | Odd              |
| 1                    | 1 | 1 | 0 | 0 | 0 | 0                | 1 | 8         | Even             |
| 1                    | 1 | 1 | 0 | 0 | 0 | 1                | 0 | 8         | None             |

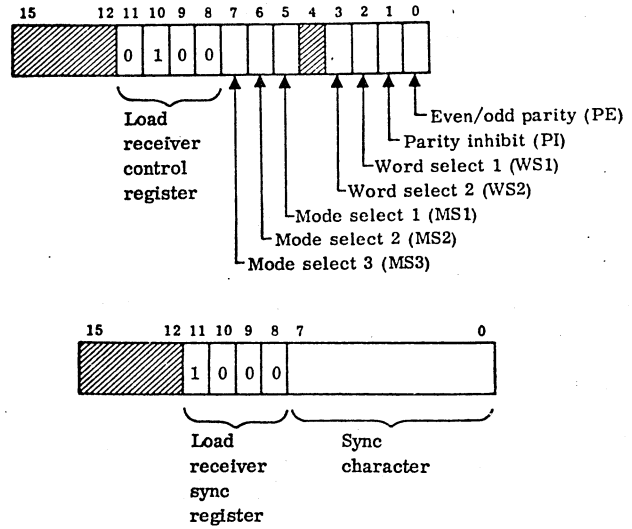
†WS2 is MSB; PE is LSB.

### Transmitter Control Word Format

| Control Word Format† |   |   |   |   |   | Character Format |   |            |                  |               |
|----------------------|---|---|---|---|---|------------------|---|------------|------------------|---------------|
| W                    | W | M | M | C | C | P                | P | Data Bits  | Added Parity Bit | Stop Elements |
| 2                    | 1 | 2 | 1 | 2 | 1 |                  |   |            |                  |               |
| 7                    | 6 | 5 | 4 | 3 | 2 | 1                | 0 |            |                  |               |
| 0                    | 0 | 0 | 0 | 1 | 1 | 0                | 0 | 5          | Odd              | 1             |
| 0                    | 0 | 0 | 1 | 1 | 1 | 0                | 0 | 5          | Odd              | 1,5           |
| 0                    | 0 | 0 | 0 | 1 | 1 | 0                | 1 | 5          | Even             | 1             |
| 0                    | 0 | 0 | 1 | 1 | 1 | 0                | 1 | 5          | Even             | 1,5           |
| 0                    | 0 | 0 | 0 | 1 | 1 | 1                | 0 | 5          | None             | 1             |
| 0                    | 0 | 0 | 1 | 1 | 1 | 1                | 0 | 5          | None             | 1,5           |
| 0                    | 1 | 0 | 0 | 1 | 1 | 0                | 0 | 6          | Odd              | 1             |
| 0                    | 1 | 0 | 1 | 1 | 1 | 0                | 0 | 6          | Odd              | 2             |
| 0                    | 1 | 0 | 0 | 1 | 1 | 0                | 1 | 6          | Even             | 1             |
| 0                    | 1 | 0 | 1 | 1 | 1 | 0                | 1 | 6          | Even             | 2             |
| 0                    | 1 | 0 | 0 | 1 | 1 | 1                | 0 | 6          | None             | 1             |
| 0                    | 1 | 0 | 1 | 1 | 1 | 1                | 0 | 6          | None             | 2             |
| 1                    | 0 | 0 | 0 | 1 | 1 | 0                | 0 | 7          | Odd              | 1             |
| 1                    | 0 | 0 | 1 | 1 | 1 | 0                | 0 | 7          | Odd              | 2             |
| 1                    | 0 | 0 | 0 | 1 | 1 | 0                | 1 | 7          | Even             | 1             |
| 1                    | 0 | 0 | 1 | 1 | 1 | 0                | 1 | 7          | Even             | 2             |
| 1                    | 0 | 0 | 0 | 1 | 1 | 1                | 0 | 7          | None             | 1             |
| 1                    | 0 | 0 | 1 | 1 | 1 | 1                | 0 | 7          | None             | 2             |
| 1                    | 1 | 0 | 0 | 1 | 1 | 0                | 0 | 8          | Odd              | 1             |
| 1                    | 1 | 0 | 1 | 1 | 1 | 0                | 0 | 8          | Odd              | 2             |
| 1                    | 1 | 0 | 0 | 1 | 1 | 0                | 1 | 8          | Even             | 1             |
| 1                    | 1 | 0 | 1 | 1 | 1 | 0                | 1 | 8          | Even             | 2             |
| 1                    | 1 | 0 | 0 | 1 | 1 | 1                | 0 | 8          | None             | 1             |
| 1                    | 1 | 0 | 1 | 1 | 1 | 1                | 0 | 8          | None             | 2             |
| X                    | X | X | X | 1 | 0 | X                | X | 19.2K baud |                  |               |

†WS2 is MSB; PE is LSB.

Notes: 1. First bit is always 1 and is the start bit.  
2. Bit 2 of transmitter control word must be 0 for operation at 19.2K baud.



### Receiver Control Word Format for Synchronous Operation

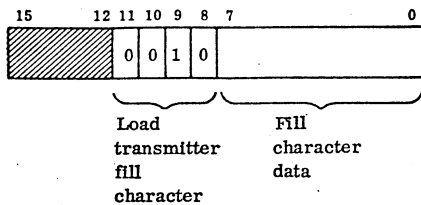
| Control Word Format† |   |   |   |   |           | Character Format |   |   |      |
|----------------------|---|---|---|---|-----------|------------------|---|---|------|
| R                    | R | R | W | W | Data Bits | Added Parity Bit |   |   |      |
| 3                    | 2 | 1 | 2 | 1 |           |                  |   |   |      |
| 7                    | 6 | 5 | 4 | 3 | 2         | 1                | 0 |   |      |
| 1                    | 0 | 1 | X | 0 | 0         | 0                | 0 | 5 | Odd  |
| 1                    | 0 | 1 | X | 0 | 0         | 0                | 1 | 5 | Even |
| 1                    | 0 | 1 | X | 0 | 0         | 1                | 0 | 5 | None |
| 1                    | 0 | 1 | X | 0 | 1         | 0                | 0 | 6 | Odd  |
| 1                    | 0 | 1 | X | 0 | 1         | 0                | 1 | 6 | Even |
| 1                    | 0 | 1 | X | 0 | 1         | 1                | 0 | 6 | None |
| 1                    | 0 | 1 | X | 1 | 0         | 0                | 0 | 7 | Odd  |
| 1                    | 0 | 1 | X | 1 | 0         | 0                | 1 | 7 | Even |
| 1                    | 0 | 1 | X | 1 | 0         | 1                | 0 | 7 | None |
| 1                    | 0 | 1 | X | 1 | 1         | 0                | 0 | 8 | Odd  |
| 1                    | 0 | 1 | X | 1 | 1         | 0                | 1 | 8 | Even |
| 1                    | 0 | 1 | X | 1 | 1         | 1                | 0 | 8 | None |

†RMS3 is MSB; PE is LSB.

Note: X = Bit not sampled

### EXTENDED CHANNEL CONTROL RECEIVER

#### A Register



Receiver Control Word Format  
for Asynchronous Operation

| Control Word Format† |   |   |       |   |   |       |   |   |       | Character Format |           |                  |               |
|----------------------|---|---|-------|---|---|-------|---|---|-------|------------------|-----------|------------------|---------------|
| R R R                |   |   | S S S |   |   | M M M |   |   | 3 2 1 | Start Bit        | Data Bits | Added Parity Bit | Stop Elements |
| 7                    | 6 | 5 | 4     | 3 | 2 | 1     | 0 |   |       |                  |           |                  |               |
| 0                    | 1 | 1 | X     | 0 | 0 | 0     | 0 | 1 | 5     | Odd              | 1 or more |                  |               |
| 0                    | 1 | 1 | X     | 0 | 0 | 0     | 1 | 1 | 5     | Even             | 1 or more |                  |               |
| 0                    | 1 | 1 | X     | 0 | 0 | 1     | 0 | 1 | 5     | None             | 1 or more |                  |               |
| 0                    | 1 | 1 | X     | 0 | 1 | 0     | 0 | 1 | 6     | Odd              | 1 or more |                  |               |
| 0                    | 1 | 1 | X     | 0 | 1 | 0     | 1 | 1 | 6     | Even             | 1 or more |                  |               |
| 0                    | 1 | 1 | X     | 0 | 1 | 1     | 0 | 1 | 6     | None             | 1 or more |                  |               |
| 0                    | 1 | 1 | X     | 1 | 0 | 0     | 0 | 1 | 7     | Odd              | 1 or more |                  |               |
| 0                    | 1 | 1 | X     | 1 | 0 | 0     | 1 | 1 | 7     | Even             | 1 or more |                  |               |
| 0                    | 1 | 1 | X     | 1 | 0 | 1     | 0 | 1 | 7     | None             | 1 or more |                  |               |
| 0                    | 1 | 1 | X     | 1 | 1 | 0     | 0 | 1 | 8     | Odd              | 1 or more |                  |               |
| 0                    | 1 | 1 | X     | 1 | 1 | 0     | 1 | 1 | 8     | Even             | 1 or more |                  |               |
| 0                    | 1 | 1 | X     | 1 | 1 | 1     | 0 | 1 | 8     | None             | 1 or more |                  |               |

†RMS3 is MSB; 0 is LSB.

Notes: 1. X = Bit not sampled  
2. For 19.2K baud operation, bit 5 of the receiver control word must be 0.

MAGNETIC TAPE CONTROLLER (LCTT)

FUNCTION WITH SET I/O

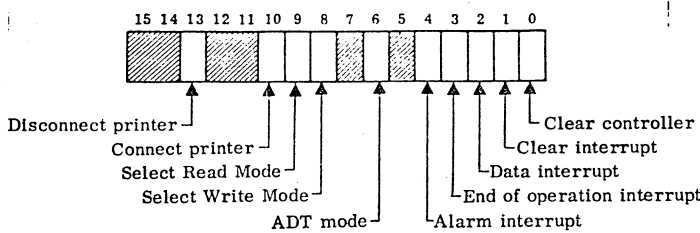
Q Register

|    |    |    |   |   |   |             |          |      |   |
|----|----|----|---|---|---|-------------|----------|------|---|
| 15 | 11 | 10 | 9 | 7 | 6 | 4           | 3        | 1    | 0 |
| 0  | 0  | 0  | 0 | 0 | 1 | EQUIPT. NO. | POSITION | MODE | 0 |

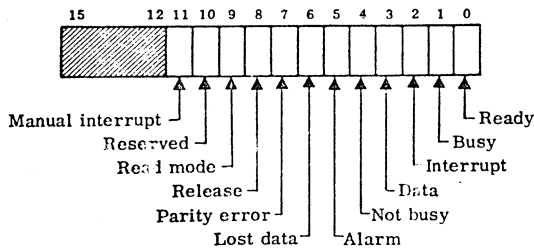
| Bits                | Meaning                                                                                                                                                                                                              |
|---------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0 and 11 through 15 | Must be zero.                                                                                                                                                                                                        |
| 1 through 3         | Specifies mode in which device is to operate. When bit 3 is 1, one data word is set (output) from the A register. When bit 3 is zero, one data word is sampled (input to the A register). Bits 1 and 2 are not used. |
| 4 through 6         | Not used                                                                                                                                                                                                             |
| 7 through 9         | Specifies the equipment number of the device                                                                                                                                                                         |
| 10                  | Must be one                                                                                                                                                                                                          |

CDT/TTY

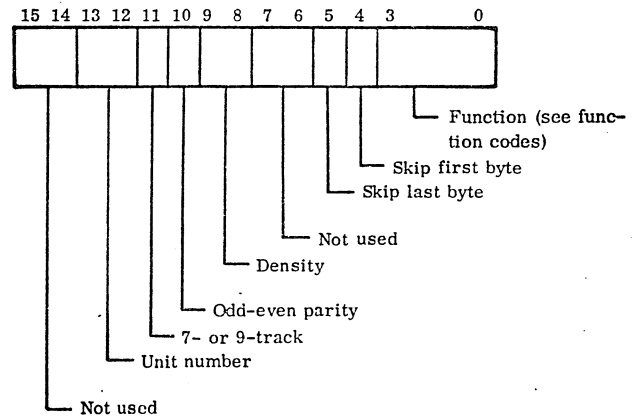
DIRECTOR FUNCTION



DIRECTOR STATUS



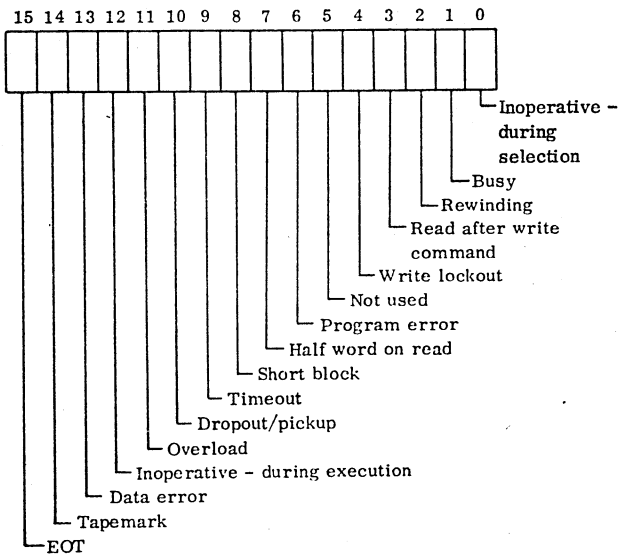
A Register





STATUS ASSIGNMENTS

A Register



- NOTES: 1. Bits 0 through 4 are the intermediate status.  
2. Bits 5 through 15 are the terminating status.

TABLE 5. FUNCTION CONTROL REGISTER (FCR)

| Bit      | Digit | Bit Definition                                                                                                                                                                        |
|----------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31       | 1F    | Overflow<br>Not Protected Instruction<br>Protect Fault<br>Parity Error<br>Status Only                                                                                                 |
| 30       | 1E    |                                                                                                                                                                                       |
| 29       | 1D    |                                                                                                                                                                                       |
| 28       | 1C    |                                                                                                                                                                                       |
| 27       | 1B    | Interrupt System Active<br>Auto-Restart Enabled<br>Micro Running<br>Macro Running<br>Status Only                                                                                      |
| 26       | 1A    |                                                                                                                                                                                       |
| 25       | 19    |                                                                                                                                                                                       |
| 24       | 18    |                                                                                                                                                                                       |
| 23       | 17    | Not used<br>Not used<br>Enable Auto Display<br>Enable Console Echo                                                                                                                    |
| 22       | 16    |                                                                                                                                                                                       |
| 21       | 15    |                                                                                                                                                                                       |
| 20       | 14    |                                                                                                                                                                                       |
| 19       | 13    | Enable Micro Memory Write<br>Multilevel Indirect Addressing Mode<br>Not used<br>Suppress Console                                                                                      |
| 18       | 12    |                                                                                                                                                                                       |
| 17       | 11    |                                                                                                                                                                                       |
| 16       | 10    |                                                                                                                                                                                       |
| 15       | 0F    | 0 0 Breakpoint Off<br>0 1 Instruction Reference BP<br>1 0 Storage Operand BP<br>1 1 All References BP<br>BP Interrupt (BP Stop if Clear)<br>Micro BP, Step, Go, Stop (Macro if Clear) |
| 14       | 0E    |                                                                                                                                                                                       |
| 13       | 0D    |                                                                                                                                                                                       |
| 12       | 0C    |                                                                                                                                                                                       |
| 11       | 0B    | Step<br>Selective Stop<br>Selective Skip<br>Protect Switch                                                                                                                            |
| 10       | 0A    |                                                                                                                                                                                       |
| 09       | 09    |                                                                                                                                                                                       |
| 08       | 08    |                                                                                                                                                                                       |
| 07       | 07    | DISPLAY 1                                                                                                                                                                             |
| 06       | 06    |                                                                                                                                                                                       |
| 05       | 05    |                                                                                                                                                                                       |
| 04       | 04    |                                                                                                                                                                                       |
| 03       | 03    | DISPLAY 1                                                                                                                                                                             |
| 02       | 02    |                                                                                                                                                                                       |
| 01       | 01    |                                                                                                                                                                                       |
| (MSB) 00 | 00    |                                                                                                                                                                                       |

## DISPLAY CODE DEFINITIONS

| Code      | Select Code | Display 0<br>(L Function)                | Select Code | Display 1<br>(K Function)    |
|-----------|-------------|------------------------------------------|-------------|------------------------------|
| 0 0 0 0 0 | J00:        | F2 (addressed by N)                      | J10:        | FCR                          |
| 1 0 0 0 1 | J01:        | N (two MSDs)                             | J11:        | P (1)                        |
| 2 0 0 1 0 | J02:        | K (two LSDs)                             | J12:        | I                            |
| 3 0 0 1 1 | J03:        | X                                        |             |                              |
| 4 0 1 0 0 | J04:        | Q                                        | J14:        | A                            |
| 5 0 1 0 1 | J05:        | F                                        | J15:        | MIR                          |
| 6 0 1 1 0 | J06:        | F1 (addressed by K;<br>enabled by SM111) | J16:        | BP-P/MA                      |
| 7 0 1 1 1 | J07:        | MEM                                      | J17:        | BP-P/MA<br>(display<br>only) |
| 8 1 0 0 0 |             |                                          | J18:        | SM1                          |
| 9 1 0 0 1 | J09:        | $\overline{RTJ}$                         | J19:        | M1                           |
| A 1 0 1 0 |             |                                          | J1A:        | SM2                          |
| B 1 0 1 1 |             |                                          | J1B:        | M2                           |
| C 1 1 0 0 | J0C:        | MM                                       |             |                              |
| D 1 1 0 1 |             |                                          | J1D:        | A*                           |
| E 1 1 1 0 |             |                                          | J1E:        | X*                           |
| F 1 1 1 1 |             |                                          | J1F:        | Q*                           |

**Notes:** 1. Used to address macro memory. Automatically incremented after each memory reference.  
 2. Combined contents of these two registers are used to address micro memory. K register automatically incremented after each memory reference. N register does not automatically increment.

# EQUIPMENT CODE, LOGICAL UNIT, AND INTERRUPT LINE TABLE G

| Device          | WES             |                   | Logical Unit | Interrupt Line |       |
|-----------------|-----------------|-------------------|--------------|----------------|-------|
|                 | Equipment Code† | Equipment Address |              | Micro          | Macro |
|                 | Card Reader     | 0581              |              | B              | 5     |
| Line Printer    | 0201            | 4                 | 3            | 4              | 4     |
| LCTT Controller | 0600            | C                 | 1            | 7              | C     |
| DCCLA           | 0500            | A                 | 6            | A              | A     |
| LIAT            | 0091            | 1                 | 4            | 1              | 1     |
| Real-Time Clock | 00F3            | 1                 | N/A          | N/A            | 8     |

†The equipment code is part of the WES.



## GENERAL DESCRIPTION

MEMDMP is a memory to printer dump using A/Q I/O. The operator sets the A register to the dump start address and the Q register to the dump end address plus 1. Then he restarts the program. The input and output format is as follows:

```
A K :
Q L :
```

It is important that A is selected first; otherwise it dumps from location O.

After the dump stops, A and Q may be changed for different dump locations. To restart the ODS diagnostic, LODCHK must be reloaded.

### NOTE

It is suggested (to dump 32K) that

```
A = 0
Q = 8000
```

## LOADING PROCEDURES

This program is loaded as a deadstart load as follows:

1. Master clear the machine.
2. Place the MEMDMP deck into the card reader hopper.
3. Press the deadstart switch.

The dump program is loaded at 1F00 for overlay systems. If a system with greater than 8K is used, the dump program should be loaded at the highest address possible. The dump program requires 100<sub>16</sub> words of memory.

## MEMDMP DEADSTART

The first and last cards of the MEMDMP deadstart deck control the address at which the MEMDMP program is deadstarted into main memory of the processor. The format of the first card is:

```
K 7 1 0 0 8 0 0 0 G K x x x x G
```

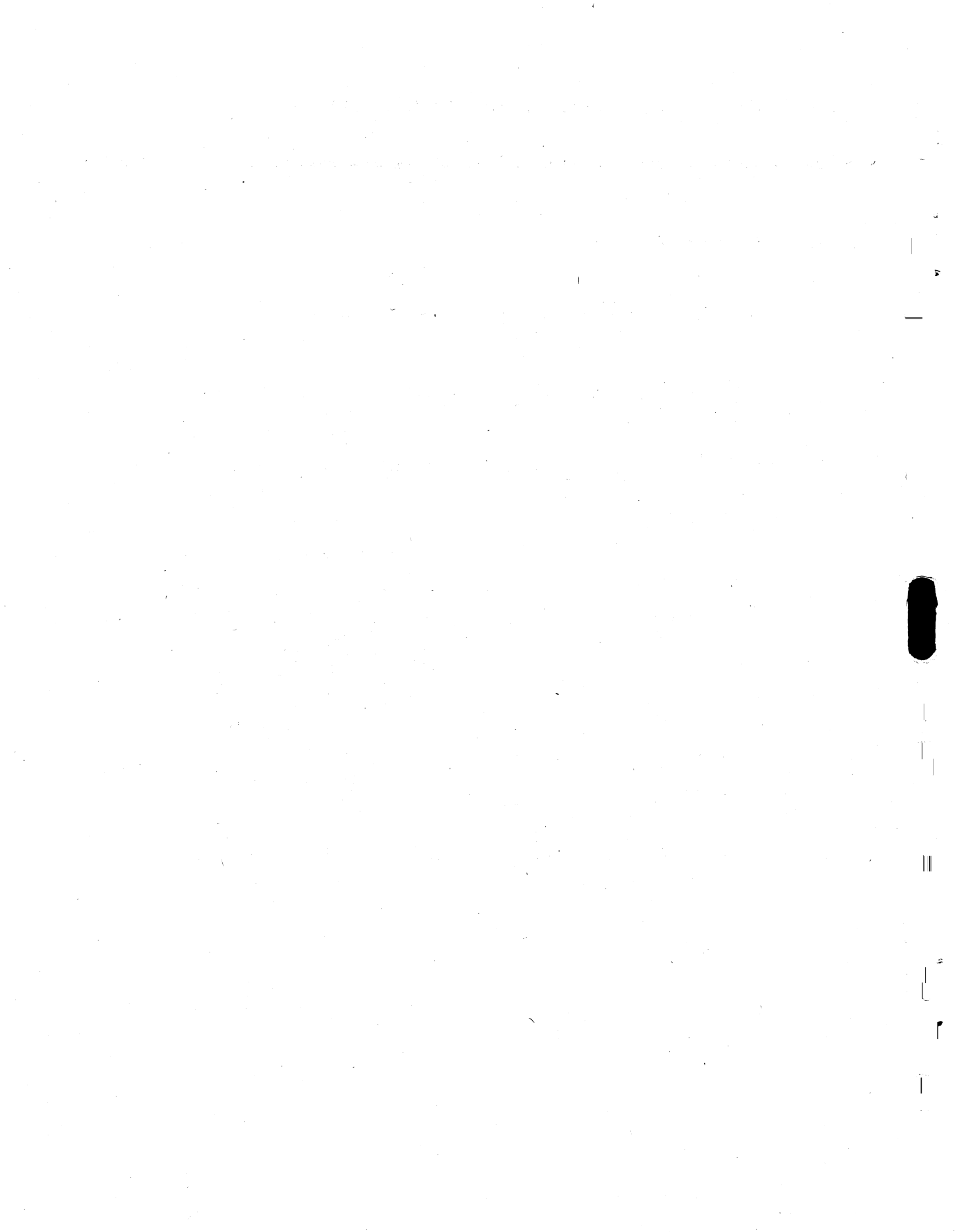
The format of the last card is:

```
K x x x x G J 1 0 G K 4 4 6 0 2 8 0 0 G
```

The parameter xxxx on both cards determines the deadstart address. The following table specifies the value for parameter xxxx for loading into the various stacks:

| Value of xxxx | No. of Stacks |
|---------------|---------------|
| 1F00          | 1             |
| 3F00          | 2             |
| 5F00          | 3             |
| 7F00          | 4             |

The default xxxx value is 1F00.



# CONVERSION TABLES

## DECIMAL/HEXADECIMAL CONVERSION TABLE

|     | 0    | 1    | 2    | 3    | 4    | 5    | 6    | 7    | 8    | 9    |      | 0    | 1    | 2    | 3    | 4    | 5    | 6    | 7    | 8    | 9    |
|-----|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|
| 0   | 0000 | 0001 | 0002 | 0003 | 0004 | 0005 | 0006 | 0007 | 0008 | 0009 | 520  | 0208 | 0209 | 020A | 020B | 020C | 020D | 020E | 020F | 0210 | 0211 |
| 10  | 000A | 000B | 000C | 000D | 000E | 000F | 0010 | 0011 | 0012 | 0013 | 530  | 0212 | 0213 | 0214 | 0215 | 0216 | 0217 | 0218 | 0219 | 021A | 021B |
| 20  | 0014 | 0015 | 0016 | 0017 | 0018 | 0019 | 001A | 001B | 001C | 001D | 540  | 021C | 021D | 021E | 021F | 0220 | 0221 | 0222 | 0223 | 0224 | 0225 |
| 30  | 001E | 001F | 0020 | 0021 | 0022 | 0023 | 0024 | 0025 | 0026 | 0027 | 550  | 0226 | 0227 | 0228 | 0229 | 022A | 022B | 022C | 022D | 022E | 022F |
| 40  | 0028 | 0029 | 002A | 002B | 002C | 002D | 002E | 002F | 0030 | 0031 | 560  | 0230 | 0231 | 0232 | 0233 | 0234 | 0235 | 0236 | 0237 | 0238 | 0239 |
| 50  | 0032 | 0033 | 0034 | 0035 | 0036 | 0037 | 0038 | 0039 | 003A | 003B | 570  | 023A | 023B | 023C | 023D | 023E | 023F | 0240 | 0241 | 0242 | 0243 |
| 60  | 003C | 003D | 003E | 003F | 0040 | 0041 | 0042 | 0043 | 0044 | 0045 | 580  | 0244 | 0245 | 0246 | 0247 | 0248 | 0249 | 024A | 024B | 024C | 024D |
| 70  | 0046 | 0047 | 0048 | 0049 | 004A | 004B | 004C | 004D | 004E | 004F | 590  | 024E | 024F | 0250 | 0251 | 0252 | 0253 | 0254 | 0255 | 0256 | 0257 |
| 80  | 0050 | 0051 | 0052 | 0053 | 0054 | 0055 | 0056 | 0057 | 0058 | 0059 | 600  | 0258 | 0259 | 025A | 025B | 025C | 025D | 025E | 025F | 0260 | 0261 |
| 90  | 005A | 005B | 005C | 005D | 005E | 005F | 0060 | 0061 | 0062 | 0063 | 610  | 0262 | 0263 | 0264 | 0265 | 0266 | 0267 | 0268 | 0269 | 026A | 026B |
| 100 | 0064 | 0065 | 0066 | 0067 | 0068 | 0069 | 006A | 006B | 006C | 006D | 620  | 026C | 026D | 026E | 026F | 0270 | 0271 | 0272 | 0273 | 0274 | 0275 |
| 110 | 006E | 006F | 0070 | 0071 | 0072 | 0073 | 0074 | 0075 | 0076 | 0077 | 630  | 0276 | 0277 | 0278 | 0279 | 027A | 027B | 027C | 027D | 027E | 027F |
| 120 | 0078 | 0079 | 007A | 007B | 007C | 007D | 007E | 007F | 0080 | 0081 | 640  | 0280 | 0281 | 0282 | 0283 | 0284 | 0285 | 0286 | 0287 | 0288 | 0289 |
| 130 | 0082 | 0083 | 0084 | 0085 | 0086 | 0087 | 0088 | 0089 | 008A | 008B | 650  | 028A | 028B | 028C | 028D | 028E | 028F | 0290 | 0291 | 0292 | 0293 |
| 140 | 008C | 008D | 008E | 008F | 0090 | 0091 | 0092 | 0093 | 0094 | 0095 | 660  | 0294 | 0295 | 0296 | 0297 | 0298 | 0299 | 029A | 029B | 029C | 029D |
| 150 | 0096 | 0097 | 0098 | 0099 | 009A | 009B | 009C | 009D | 009E | 009F | 670  | 029E | 029F | 02A0 | 02A1 | 02A2 | 02A3 | 02A4 | 02A5 | 02A6 | 02A7 |
| 160 | 00A0 | 00A1 | 00A2 | 00A3 | 00A4 | 00A5 | 00A6 | 00A7 | 00A8 | 00A9 | 680  | 02AB | 02A9 | 02AA | 02AB | 02AC | 02AD | 02AE | 02AF | 02B0 | 02B1 |
| 170 | 00AA | 00AB | 00AC | 00AD | 00AE | 00AF | 00B0 | 00B1 | 00B2 | 00B3 | 690  | 02B2 | 02B3 | 02B4 | 02B5 | 02B6 | 02B7 | 02B8 | 02B9 | 02BA | 02BB |
| 180 | 00B4 | 00B5 | 00B6 | 00B7 | 00B8 | 00B9 | 00BA | 00BB | 00BC | 00BD | 700  | 02BC | 02BD | 02BE | 02BF | 02C0 | 02C1 | 02C2 | 02C3 | 02C4 | 02C5 |
| 190 | 00BE | 00BF | 00C0 | 00C1 | 00C2 | 00C3 | 00C4 | 00C5 | 00C6 | 00C7 | 710  | 02C6 | 02C7 | 02C8 | 02C9 | 02CA | 02CB | 02CC | 02CD | 02CE | 02CF |
| 200 | 00C8 | 00C9 | 00CA | 00CB | 00CC | 00CD | 00CE | 00CF | 00D0 | 00D1 | 720  | 02D0 | 02D1 | 02D2 | 02D3 | 02D4 | 02D5 | 02D6 | 02D7 | 02D8 | 02D9 |
| 210 | 00D2 | 00D3 | 00D4 | 00D5 | 00D6 | 00D7 | 00D8 | 00D9 | 00DA | 00DB | 730  | 02DA | 02DB | 02DC | 02DD | 02DE | 02DF | 02E0 | 02E1 | 02E2 | 02E3 |
| 220 | 00DC | 00DD | 00DE | 00DF | 00E0 | 00E1 | 00E2 | 00E3 | 00E4 | 00E5 | 740  | 02E4 | 02E5 | 02E6 | 02E7 | 02E8 | 02E9 | 02EA | 02EB | 02EC | 02ED |
| 230 | 00E6 | 00E7 | 00E8 | 00E9 | 00EA | 00EB | 00EC | 00ED | 00EE | 00EF | 750  | 02EE | 02EF | 02F0 | 02F1 | 02F2 | 02F3 | 02F4 | 02F5 | 02F6 | 02F7 |
| 240 | 00F0 | 00F1 | 00F2 | 00F3 | 00F4 | 00F5 | 00F6 | 00F7 | 00F8 | 00F9 | 760  | 02F8 | 02F9 | 02FA | 02FB | 02FC | 02FD | 02FE | 02FF | 0300 | 0301 |
| 250 | 00FA | 00FB | 00FC | 00FD | 00FE | 00FF | 0100 | 0101 | 0102 | 0103 | 770  | 0302 | 0303 | 0304 | 0305 | 0306 | 0307 | 0308 | 0309 | 030A | 030B |
| 260 | 0104 | 0105 | 0106 | 0107 | 0108 | 0109 | 010A | 010B | 010C | 010D | 780  | 030C | 030D | 030E | 030F | 0310 | 0311 | 0312 | 0313 | 0314 | 0315 |
| 270 | 010E | 010F | 0110 | 0111 | 0112 | 0113 | 0114 | 0115 | 0116 | 0117 | 790  | 0316 | 0317 | 0318 | 0319 | 031A | 031B | 031C | 031D | 031E | 031F |
| 280 | 0118 | 0119 | 011A | 011B | 011C | 011D | 011E | 011F | 0120 | 0121 | 800  | 0320 | 0321 | 0322 | 0323 | 0324 | 0325 | 0326 | 0327 | 0328 | 0329 |
| 290 | 0122 | 0123 | 0124 | 0125 | 0126 | 0127 | 0128 | 0129 | 012A | 012B | 810  | 032A | 032B | 032C | 032D | 032E | 032F | 0330 | 0331 | 0332 | 0333 |
| 300 | 012C | 012D | 012E | 012F | 0130 | 0131 | 0132 | 0133 | 0134 | 0135 | 820  | 0334 | 0335 | 0336 | 0337 | 0338 | 0339 | 033A | 033B | 033C | 033D |
| 310 | 0136 | 0137 | 0138 | 0139 | 013A | 013B | 013C | 013D | 013E | 013F | 830  | 033E | 033F | 0340 | 0341 | 0342 | 0343 | 0344 | 0345 | 0346 | 0347 |
| 320 | 0140 | 0141 | 0142 | 0143 | 0144 | 0145 | 0146 | 0147 | 0148 | 0149 | 840  | 0348 | 0349 | 034A | 034B | 034C | 034D | 034E | 034F | 0350 | 0351 |
| 330 | 014A | 014B | 014C | 014D | 014E | 014F | 0150 | 0151 | 0152 | 0153 | 850  | 0352 | 0353 | 0354 | 0355 | 0356 | 0357 | 0358 | 0359 | 035A | 035B |
| 340 | 0154 | 0155 | 0156 | 0157 | 0158 | 0159 | 015A | 015B | 015C | 015D | 860  | 035C | 035D | 035E | 035F | 0360 | 0361 | 0362 | 0363 | 0364 | 0365 |
| 350 | 015E | 015F | 0160 | 0161 | 0162 | 0163 | 0164 | 0165 | 0166 | 0167 | 870  | 0366 | 0367 | 0368 | 0369 | 036A | 036B | 036C | 036D | 036E | 036F |
| 360 | 0168 | 0169 | 016A | 016B | 016C | 016D | 016E | 016F | 0170 | 0171 | 880  | 0370 | 0371 | 0372 | 0373 | 0374 | 0375 | 0376 | 0377 | 0378 | 0379 |
| 370 | 0172 | 0173 | 0174 | 0175 | 0176 | 0177 | 0178 | 0179 | 017A | 017B | 890  | 037A | 037B | 037C | 037D | 037E | 037F | 0380 | 0381 | 0382 | 0383 |
| 380 | 017C | 017D | 017E | 017F | 0180 | 0181 | 0182 | 0183 | 0184 | 0185 | 900  | 0384 | 0385 | 0386 | 0387 | 0388 | 0389 | 038A | 038B | 038C | 038D |
| 390 | 0186 | 0187 | 0188 | 0189 | 018A | 018B | 018C | 018D | 018E | 018F | 910  | 038E | 038F | 0390 | 0391 | 0392 | 0393 | 0394 | 0395 | 0396 | 0397 |
| 400 | 0190 | 0191 | 0192 | 0193 | 0194 | 0195 | 0196 | 0197 | 0198 | 0199 | 920  | 0398 | 0399 | 039A | 039B | 039C | 039D | 039E | 039F | 03A0 | 03A1 |
| 410 | 019A | 019B | 019C | 019D | 019E | 019F | 01A0 | 01A1 | 01A2 | 01A3 | 930  | 03A2 | 03A3 | 03A4 | 03A5 | 03A6 | 03A7 | 03A8 | 03A9 | 03AA | 03AB |
| 420 | 01A4 | 01A5 | 01A6 | 01A7 | 01A8 | 01A9 | 01AA | 01AB | 01AC | 01AD | 940  | 03AC | 03AD | 03AE | 03AF | 03B0 | 03B1 | 03B2 | 03B3 | 03B4 | 03B5 |
| 430 | 01AE | 01AF | 01B0 | 01B1 | 01B2 | 01B3 | 01B4 | 01B5 | 01B6 | 01B7 | 950  | 03B6 | 03B7 | 03B8 | 03B9 | 03BA | 03BB | 03BC | 03BD | 03BE | 03BF |
| 440 | 01B8 | 01B9 | 01BA | 01BB | 01BC | 01BD | 01BE | 01BF | 01C0 | 01C1 | 960  | 03C0 | 03C1 | 03C2 | 03C3 | 03C4 | 03C5 | 03C6 | 03C7 | 03C8 | 03C9 |
| 450 | 01C2 | 01C3 | 01C4 | 01C5 | 01C6 | 01C7 | 01C8 | 01C9 | 01CA | 01CB | 970  | 03CA | 03CB | 03CC | 03CD | 03CE | 03CF | 03D0 | 03D1 | 03D2 | 03D3 |
| 460 | 01CC | 01CD | 01CE | 01CF | 01D0 | 01D1 | 01D2 | 01D3 | 01D4 | 01D5 | 980  | 03D4 | 03D5 | 03D6 | 03D7 | 03D8 | 03D9 | 03DA | 03DB | 03DC | 03DD |
| 470 | 01D6 | 01D7 | 01D8 | 01D9 | 01DA | 01DB | 01DC | 01DD | 01DE | 01DF | 990  | 03DE | 03DF | 03E0 | 03E1 | 03E2 | 03E3 | 03E4 | 03E5 | 03E6 | 03E7 |
| 480 | 01E0 | 01E1 | 01E2 | 01E3 | 01E4 | 01E5 | 01E6 | 01E7 | 01E8 | 01E9 | 1000 | 03E8 | 03E9 | 03EA | 03EB | 03EC | 03ED | 03EE | 03EF | 03F0 | 03F1 |
| 490 | 01EA | 01EB | 01EC | 01ED | 01EE | 01EF | 01F0 | 01F1 | 01F2 | 01F3 |      |      |      |      |      |      |      |      |      |      |      |
| 500 | 01F4 | 01F5 | 01F6 | 01F7 | 01F8 | 01F9 | 01FA | 01FB | 01FC | 01FD |      |      |      |      |      |      |      |      |      |      |      |
| 510 | 01FE | 01FF | 0200 | 0201 | 0202 | 0203 | 0204 | 0205 | 0206 | 0207 |      |      |      |      |      |      |      |      |      |      |      |

# HEXADECIMAL ARITHMETIC MATRICES

## ADDITION

|   | 0 | 1  | 2  | 3  | 4  | 5  | 6  | 7  | 8  | 9  | A  | B  | C  | D  | E  | F  |
|---|---|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 0 | 0 | 1  | 2  | 3  | 4  | 5  | 6  | 7  | 8  | 9  | A  | B  | C  | D  | E  | F  |
| 1 | 1 | 2  | 3  | 4  | 5  | 6  | 7  | 8  | 9  | A  | B  | C  | D  | E  | F  | 10 |
| 2 | 2 | 3  | 4  | 5  | 6  | 7  | 8  | 9  | A  | B  | C  | D  | E  | F  | 10 | 11 |
| 3 | 3 | 4  | 5  | 6  | 7  | 8  | 9  | A  | B  | C  | D  | E  | F  | 10 | 11 | 12 |
| 4 | 4 | 5  | 6  | 7  | 8  | 9  | A  | B  | C  | D  | E  | F  | 10 | 11 | 12 | 13 |
| 5 | 5 | 6  | 7  | 8  | 9  | A  | B  | C  | D  | E  | F  | 10 | 11 | 12 | 13 | 14 |
| 6 | 6 | 7  | 8  | 9  | A  | B  | C  | D  | E  | F  | 10 | 11 | 12 | 13 | 14 | 15 |
| 7 | 7 | 8  | 9  | A  | B  | C  | D  | E  | F  | 10 | 11 | 12 | 13 | 14 | 15 | 16 |
| 8 | 8 | 9  | A  | B  | C  | D  | E  | F  | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 |
| 9 | 9 | A  | B  | C  | D  | E  | F  | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 |
| A | A | B  | C  | D  | E  | F  | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 |
| B | B | C  | D  | E  | F  | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 1A |
| C | C | D  | E  | F  | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 1A | 1B |
| D | D | E  | F  | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 1A | 1B | 1C |
| E | E | F  | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 1A | 1B | 1C | 1D |
| F | F | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 1A | 1B | 1C | 1D | 1E |

## SUBTRACTION

|   |                                             |
|---|---------------------------------------------|
| 1 | 1                                           |
| 2 | 2 4                                         |
| 3 | 3 6 9                                       |
| 4 | 4 8 C 10                                    |
| 5 | 5 A F 14 19                                 |
| 6 | 6 C 12 18 1E 24                             |
| 7 | 7 E 15 1C 23 2A 31                          |
| 8 | 8 10 18 20 28 30 38 40                      |
| 9 | 9 12 1B 24 2D 36 3F 48 51                   |
| A | A 14 1E 28 32 3C 46 50 5A 64                |
| B | B 16 21 2C 37 42 4D 58 63 6E 79             |
| C | C 18 24 30 3C 48 54 60 6C 78 84 90          |
| D | D 1A 27 34 41 4E 5B 68 75 82 8F 9C A9       |
| E | E 1C 2A 38 46 54 62 70 7E 8C 9A A8 B6 C4    |
| F | F 1E 2D 3C 4B 5A 69 78 87 96 A5 B4 C3 D2 E1 |

---

|  | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D | E | F |
|--|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
|--|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|

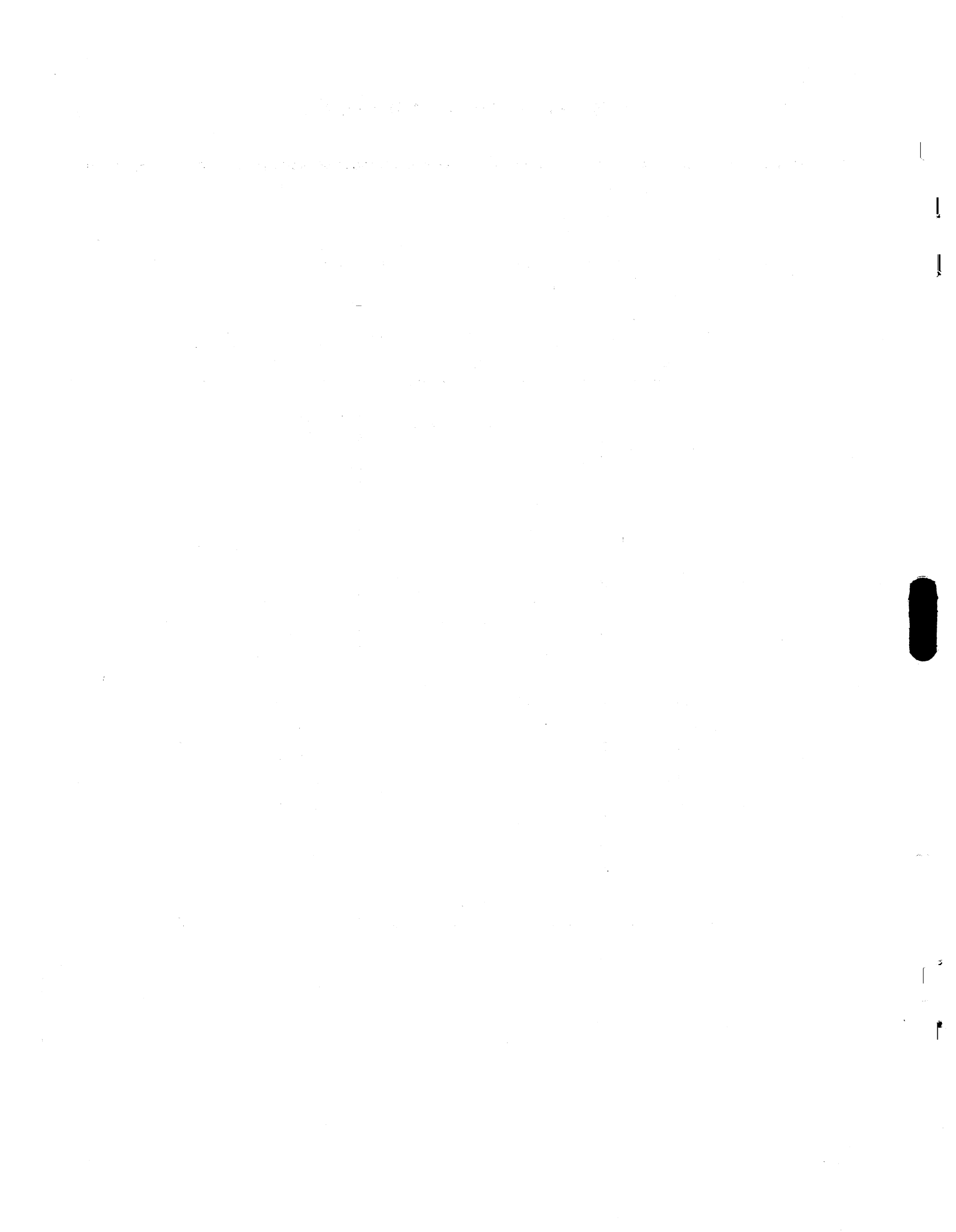
# ODS TEST TIMING AND LENGTH

All test times are based on the use of the standard default run parameters and exclude operator interface time. All test lengths listed are based on the use of

the non-overlay system. Table J-1 lists the tests, the amount of memory required for loading, and the test execution time.

TABLE J-1. MEMORY AND EXECUTION TIME REQUIRED FOR ODS TESTS

| Test Name        | Memory Required      | Execution Time |
|------------------|----------------------|----------------|
| LODCHK           | All available memory | 1 minute       |
| LDCHK2           | All available memory | 1 minute       |
| Level II Monitor | 7 K                  | N/A            |
| MPMEM            | 4.5 K                | 2-1/2 minutes  |
| MPINS            | 9 K                  | 2 minutes      |
| MPRTC            | 4 K                  | 1 minute       |
| LIAT             | 4.5 K                | 4 minutes      |
| CRECO            | 4.2 K                | 1 minute       |
| CR104            | 3 K                  | 3 minutes      |
| LP408            | 4.5 K                | 5 minutes      |
| CRUT1            | 2.5 K                | 2 minutes      |
| CRUT2            | 2.5 K                | 2 minutes      |
| LCTTA            | 1.5 K                | 1 minute       |
| LCTTB            | 8 K                  | 5 minutes      |
| CLA2A            | 6 K                  | 3 minutes      |
| C104M            | 2 K                  | 2 minutes      |
| L408M            | 2 K                  | 2 minutes      |
| CLA2M            | 2 K                  | 1 minute       |
| LCTTM            | 2 K                  | 2 minutes      |
| MEMDMP           | 3 K                  | N/A            |
| ODSBOT           | All available memory | N/A            |



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